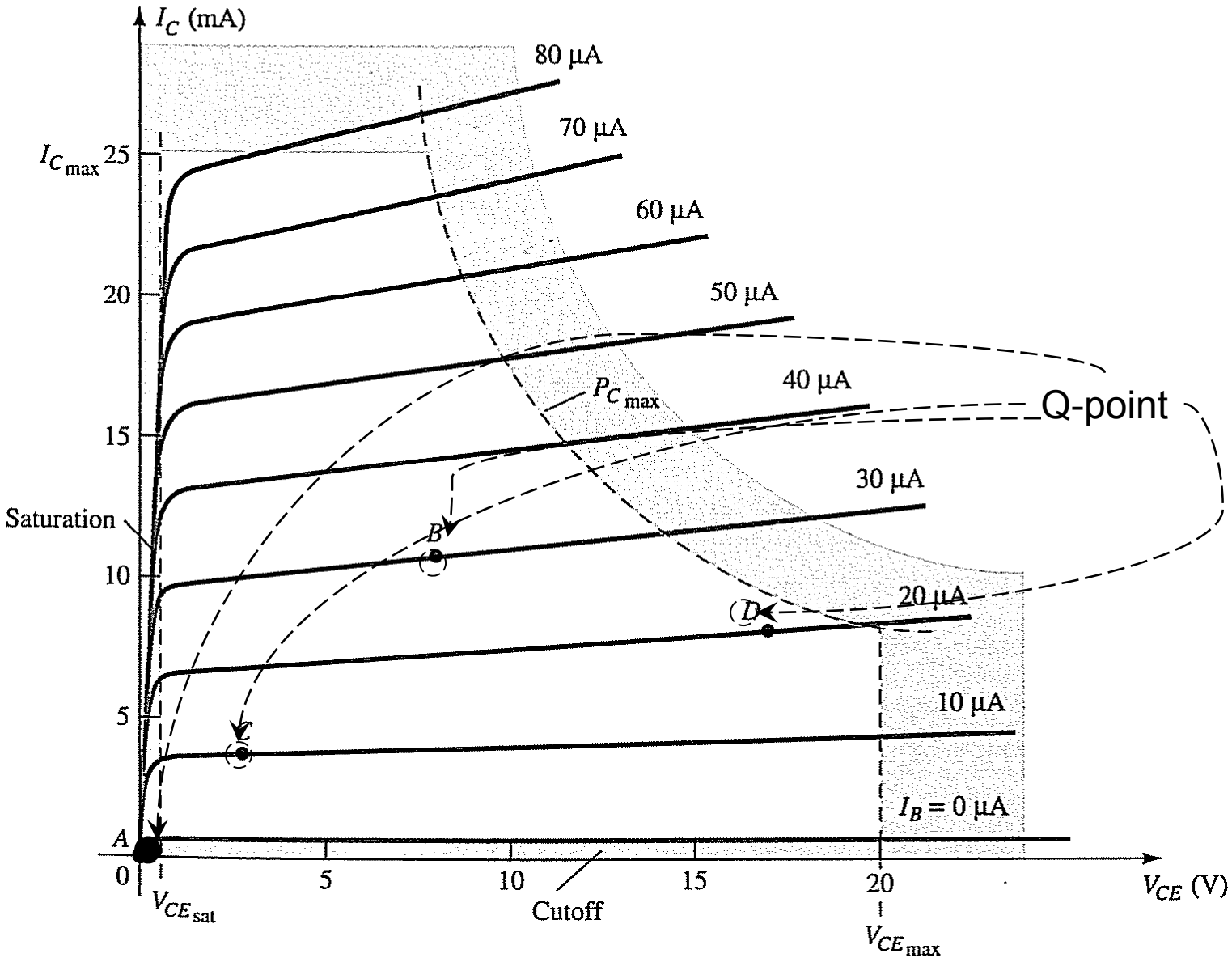
EE-110 – Basic Electronics

Bipolar Junction Transistor (BJT)

- DC Analysis

Operation Region



Operation Region

- Linear region:
  - Base-emitter junction forward-bias (V_{BE} = 0.7 V)
  - Base-collector junction reverse-bias (V_{CB})
- Cutoff region:
  - Base-emitter junction reverse-bias (V_{BE})
  - Base-collector junction reverse-bias (V_{CB})
- Saturation region:
  - Base-emitter junction forward-bias (V_{BE} = 0.7 V)
  - Base-collector junction forward-bias (V_{CB})

Recall Important Equations

$$V_{BE} = 0.7\,\text{V} \quad \text{(for npn)} \qquad V_{EB} = 0.7\,\text{V} \quad \text{(for pnp)}$$

$$I_C \approx I_E$$

$$I_C = \beta I_B$$

$$I_E = (\beta + 1) I_B$$

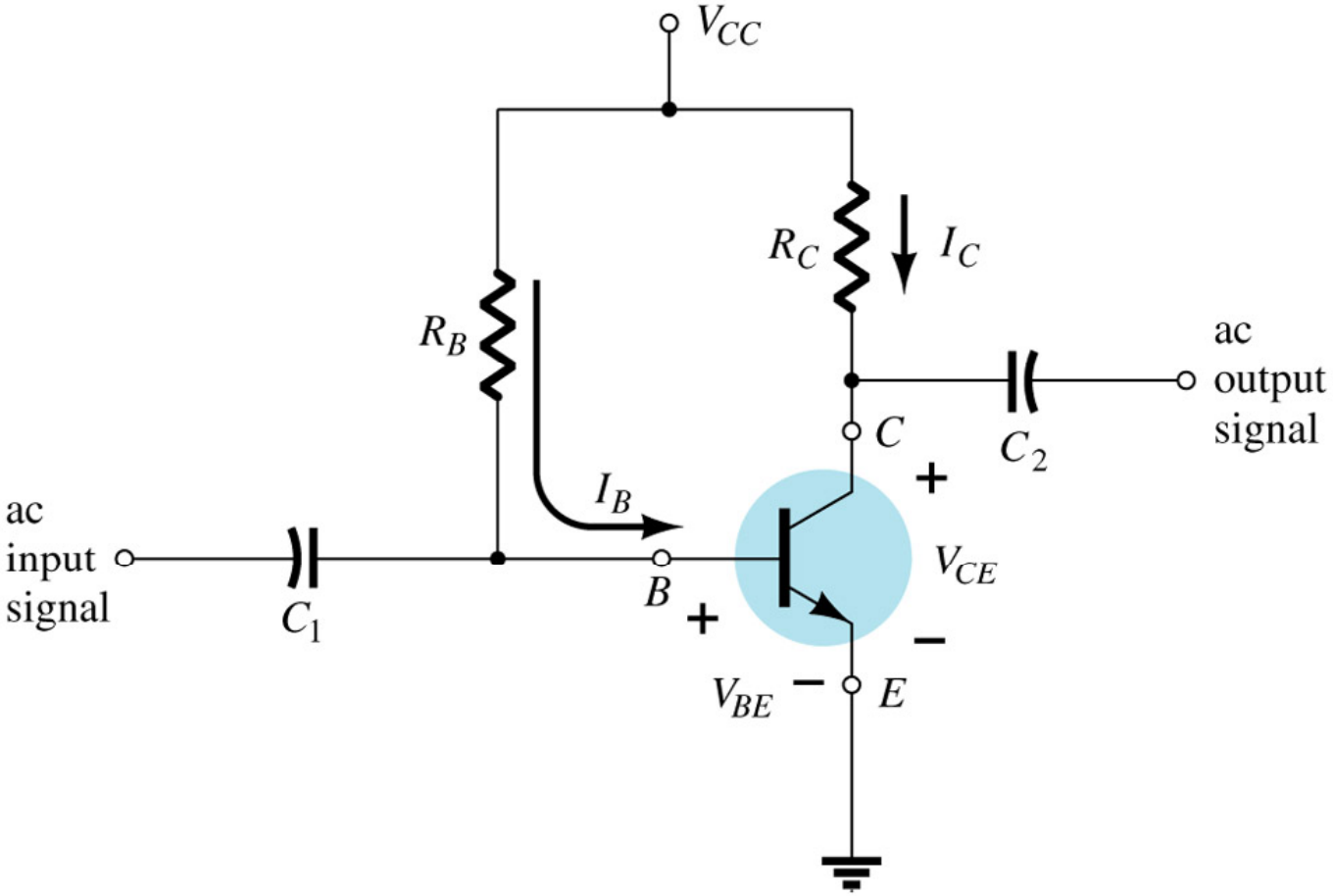
$$I_E = I_C + I_B$$

Bias Configurations

- There are many types of bias configuration
- The subtopic will cover:
  - Fixed bias configuration
  - Emitter bias configuration
  - Voltage-divider bias configuration
  - DC bias with voltage feedback configuration
  - Miscellaneous bias configuration

Fixed Bias Configuration

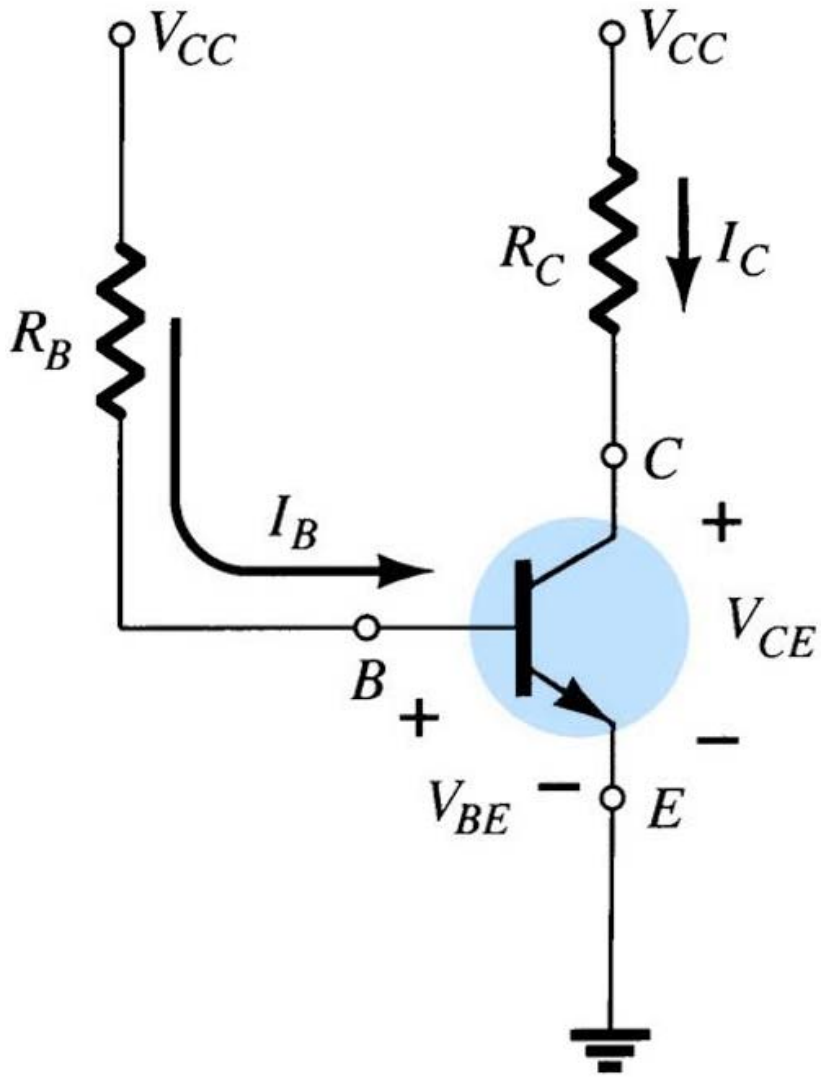
- The configuration:



Fixed Bias Configuration

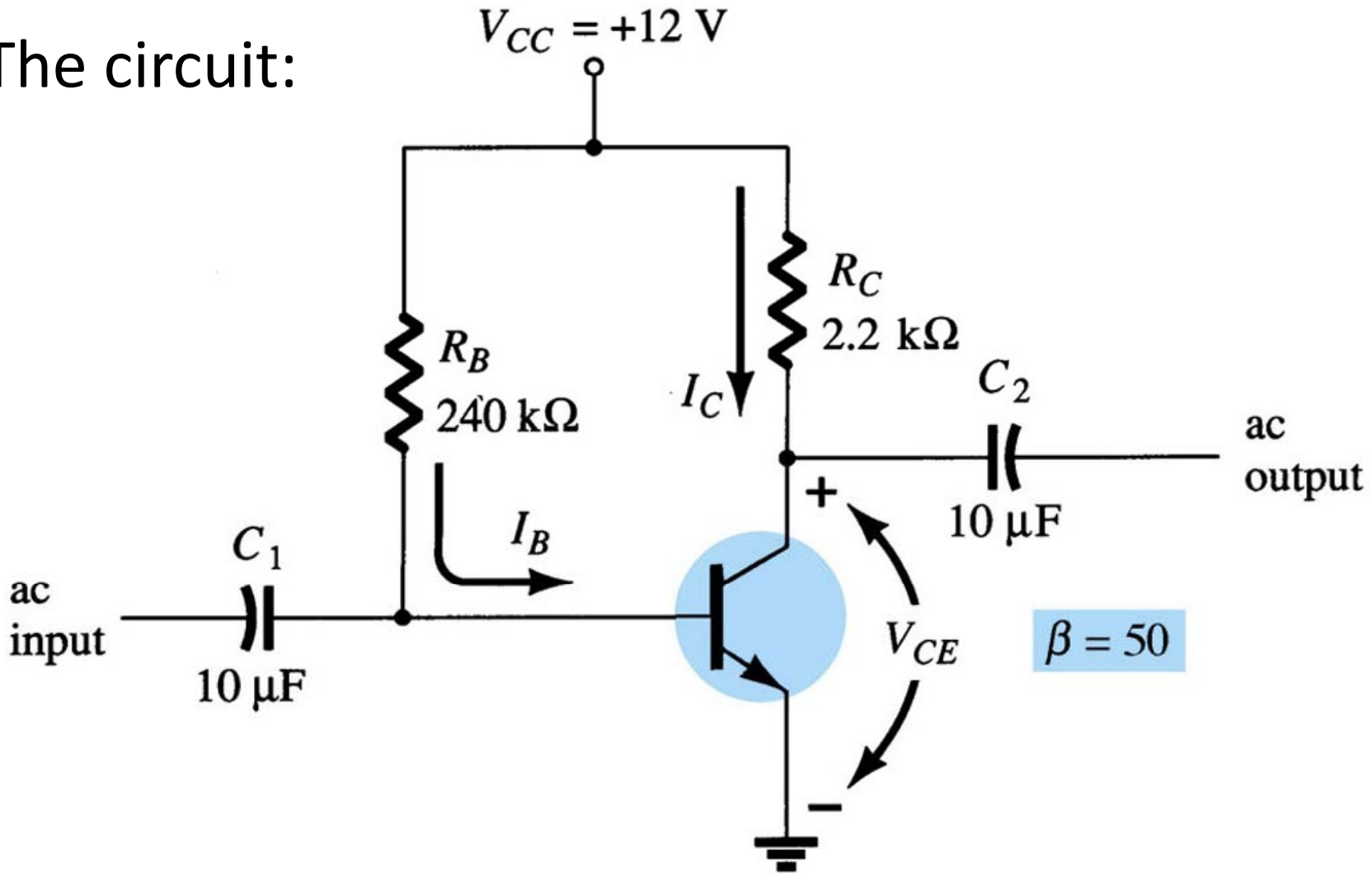
- DC equivalent circuit:
- Ignoring the ac input & output
- Ignoring the capacitor C_1 and C_2 at ac input & output terminal
- The emitter junction is grounded
- So,

$$V_E = 0$$



Example 4.1

- The circuit:



- Determine I_{BQ} and I_{CQ}
- Determine V_{CEQ}
- Determine V_B and V_C
- Determine V_{BC}

Example 4.1a

- Determine I_{BQ} and I_{CQ}:
- For I_{BQ}:

$$I_{B_Q} = I_B = \frac{V_{CC} - V_B}{R_B}$$

$$\text{where as}: V_{BE} = 0.7 = V_B - V_E$$

$$\therefore V_B = 0.7$$

$$\text{so}: I_{B_Q} = I_B = \frac{12 - 0.7}{240k} = 47.08\ \mu\text{A}$$

- For I_{CQ}:

$$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\mu) = 2.35\ \text{mA}$$

Example 4.1b

- Determine V_{CEQ}:

$$V_{CE_Q} = V_C - V_E = V_C$$

$$\text{where as}: I_C = 2.35m = \frac{V_{CC} - V_C}{R_C} =$$

$$= \frac{12 - V_C}{2.2k}$$

$$\therefore V_C = 6.83$$

$$\text{so}: V_{CE_Q} = V_C = 6.83\ \text{V}$$

Example 4.1c

- Determine V_B and V_C:
- Taken from Solution 4.1a:

$$V_B = 0.7\,\text{V}$$

$$V_C = 6.83\,\text{V}$$

Example 4.1d

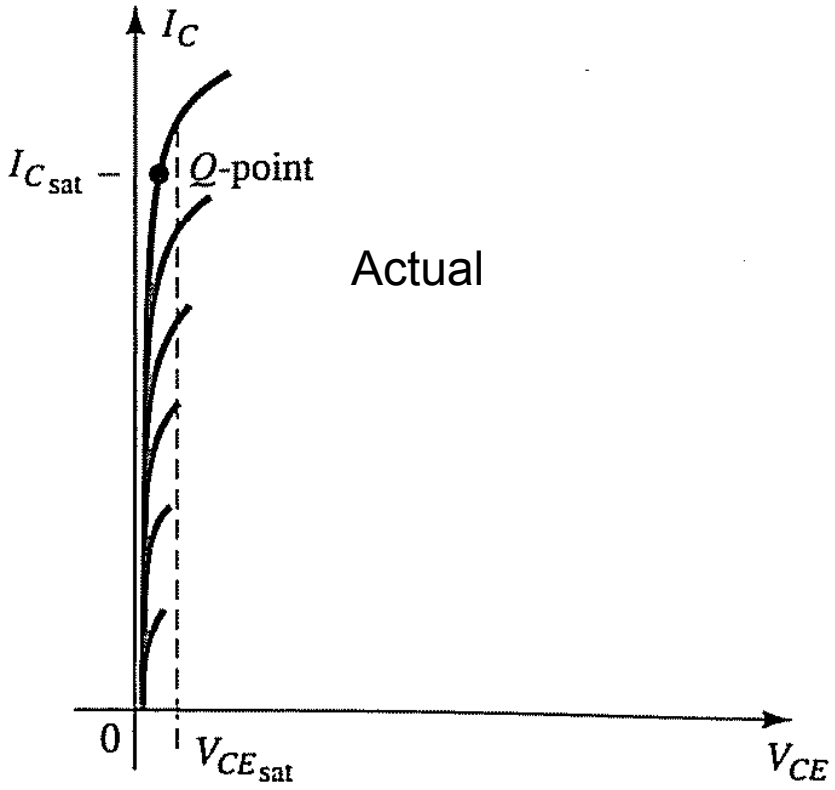
- Determine V_{BC}:

$$V_{BC} = V_B - V_C = 0.7 - 6.83 = -6.13\,\text{V}$$

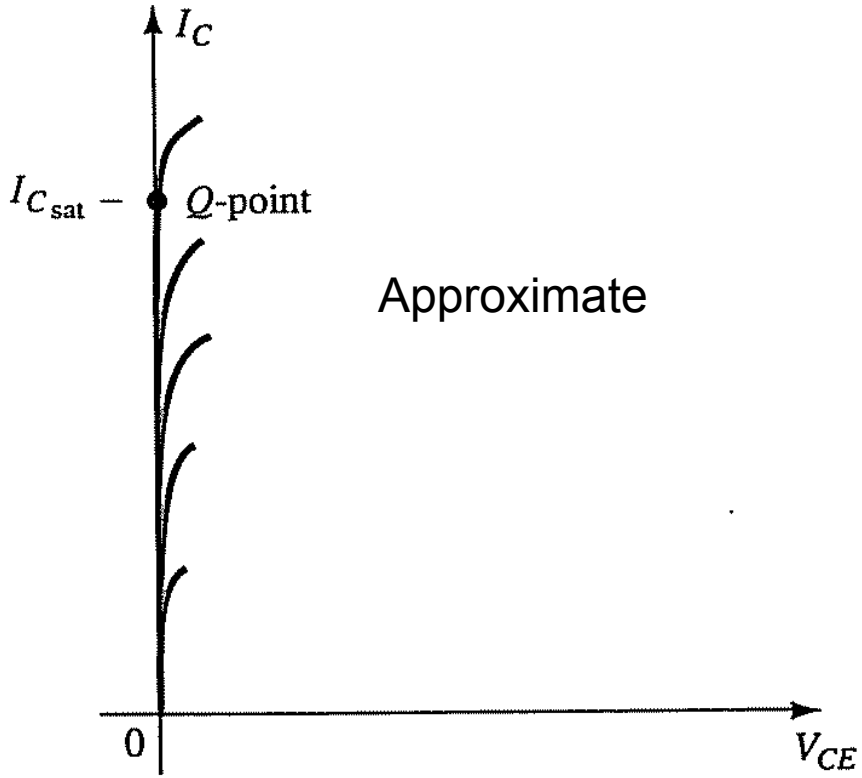
Transistor Saturation

- Saturation means for any system that have reached their maximum value
- In transistor, saturation region is where the base-collector junction is in forward bias
- When this happens, the output signal will be distorted

Transistor Saturation



Actual

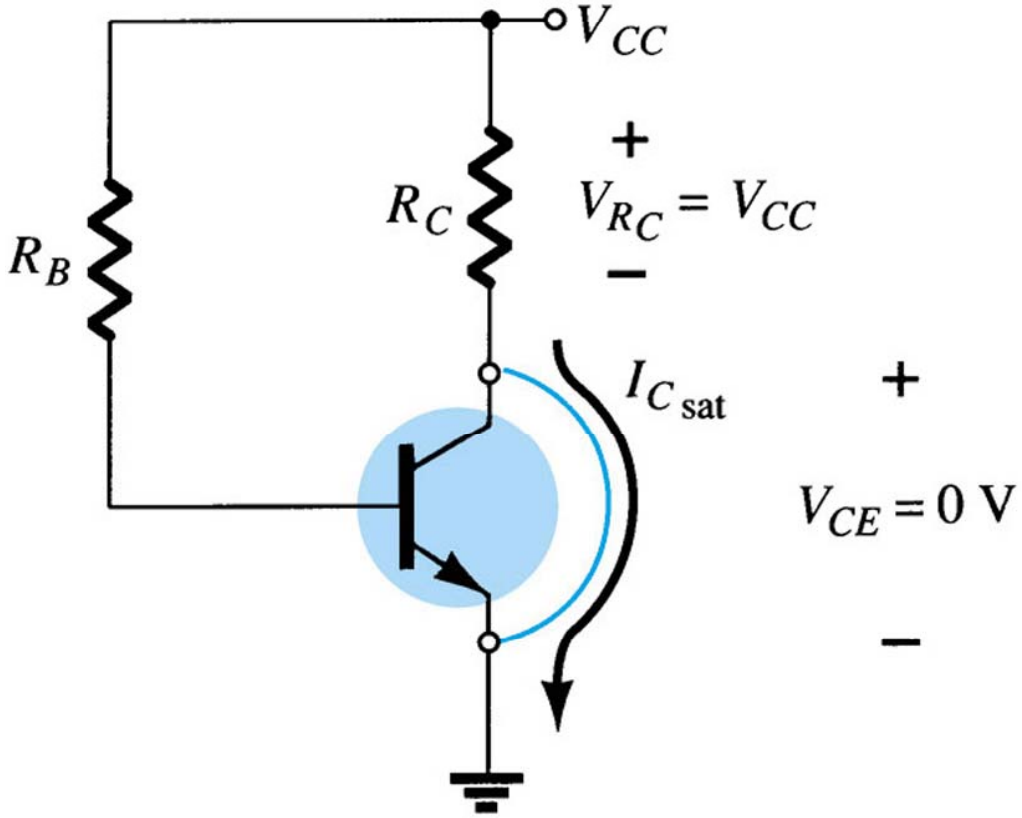


Approximate

Notice that in saturation region, $V_{CE} = 0$

Saturation Level

- For the fixed-bias configuration, to determine the saturation current, $I_{C(sat)}$, the equivalent circuit is:



Saturation Level

- The calculation:

$$V_{CE} = 0 = V_C - V_E = V_C - 0$$

$$\therefore V_C = 0$$

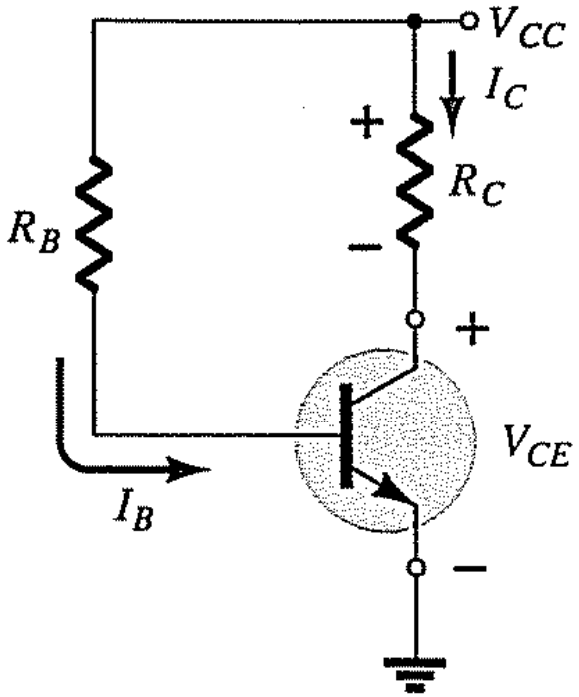
- For that, the saturation current becomes:

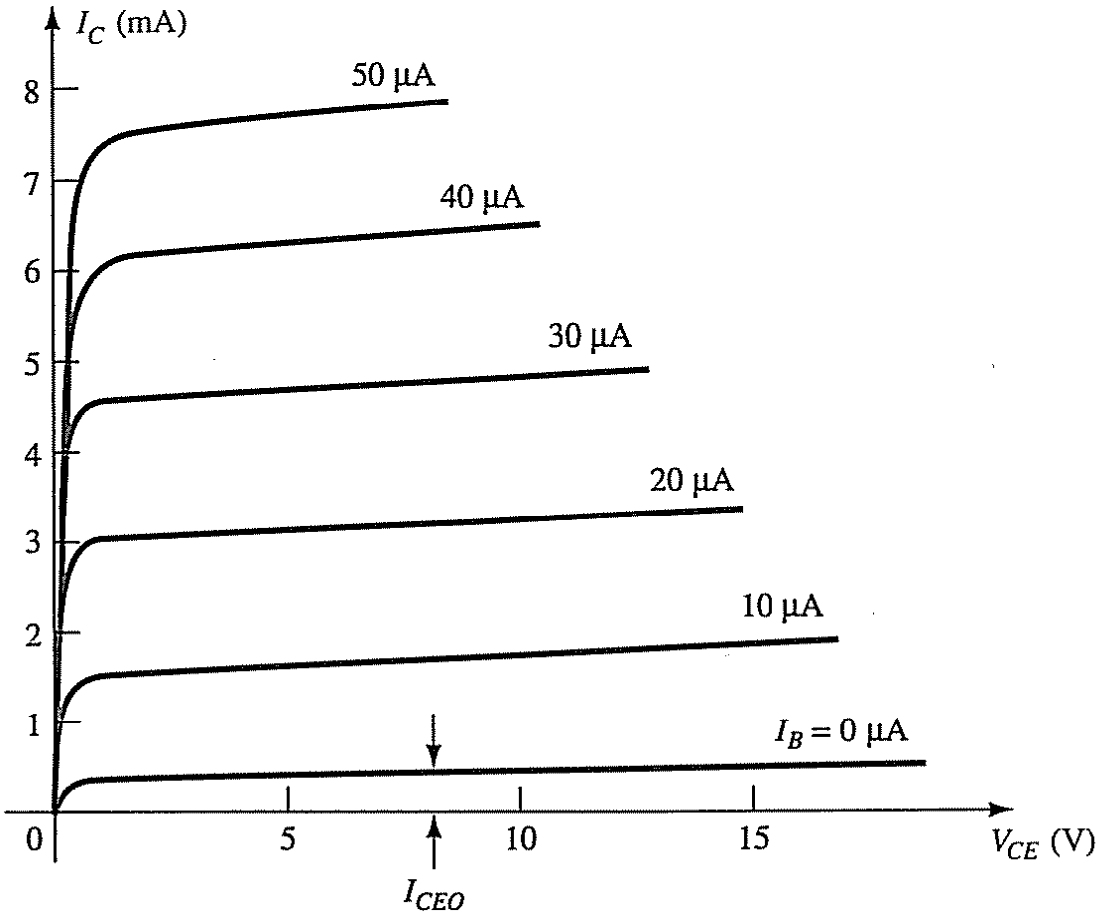
$$I_{C_{sat}} = \frac{V_{CC} - V_C}{R_C} = \frac{V_{CC} - 0}{R_C}$$

$$\therefore I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

Load-Line Analysis

- If the configuration and the device characteristic are as shown as below:





Load-Line Analysis

- A line is drawn from vertical axis to the horizontal axis (recall Load-Line Analysis for diode)
- The point from horizontal axis would be I_C = 0 (notice that the point is in cutoff-region)
- The point from vertical axis would be V_{CE} = 0 (notice that the point is in saturation-region)

Load-Line Analysis

- For $I_C = 0$:

$$I_C = \frac{V_{CC} - V_C}{R_C} = 0$$

$$\therefore V_C = V_{CC}$$

- As for $V_E = 0$:

$$V_{CE} = V_C - V_E = V_C - 0 = V_C$$

- Resulting in:

$$V_{CE} = V_{CC} \text{ (cutoff - region)}$$

Load-Line Analysis

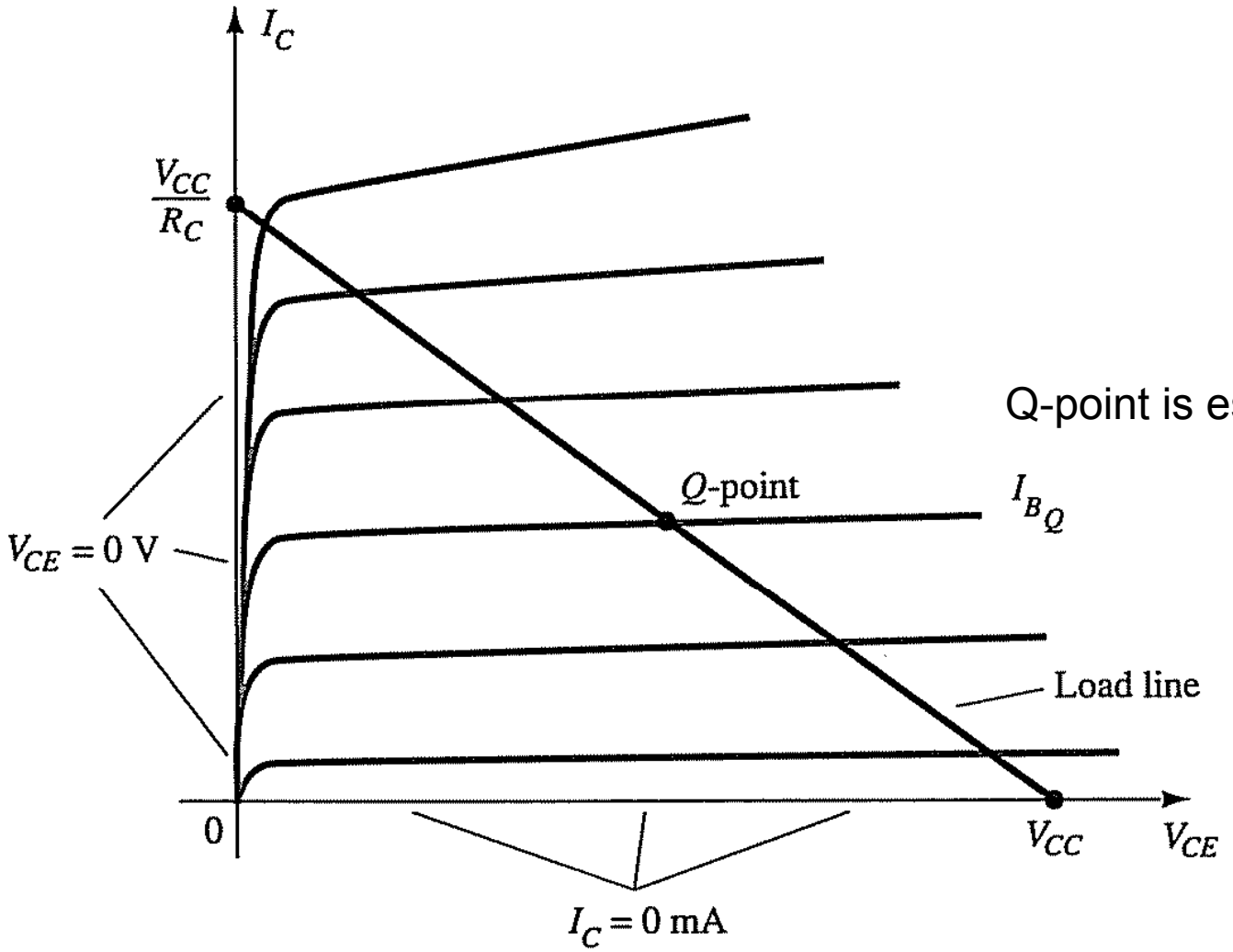
- For V_{CE} = 0, the transistor will be in saturation region
- Taking the transistor saturation equation:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

- As a conclusion, the load-line analysis for fixed-bias circuit:
  - For I_C = 0: $V_{CE} = V_{CC}$ (cutoff - region)
  - For V_{CE} = 0: $I_{C_{sat}} = \frac{V_{CC}}{R_C}$ (saturation region)

Load-Line Analysis

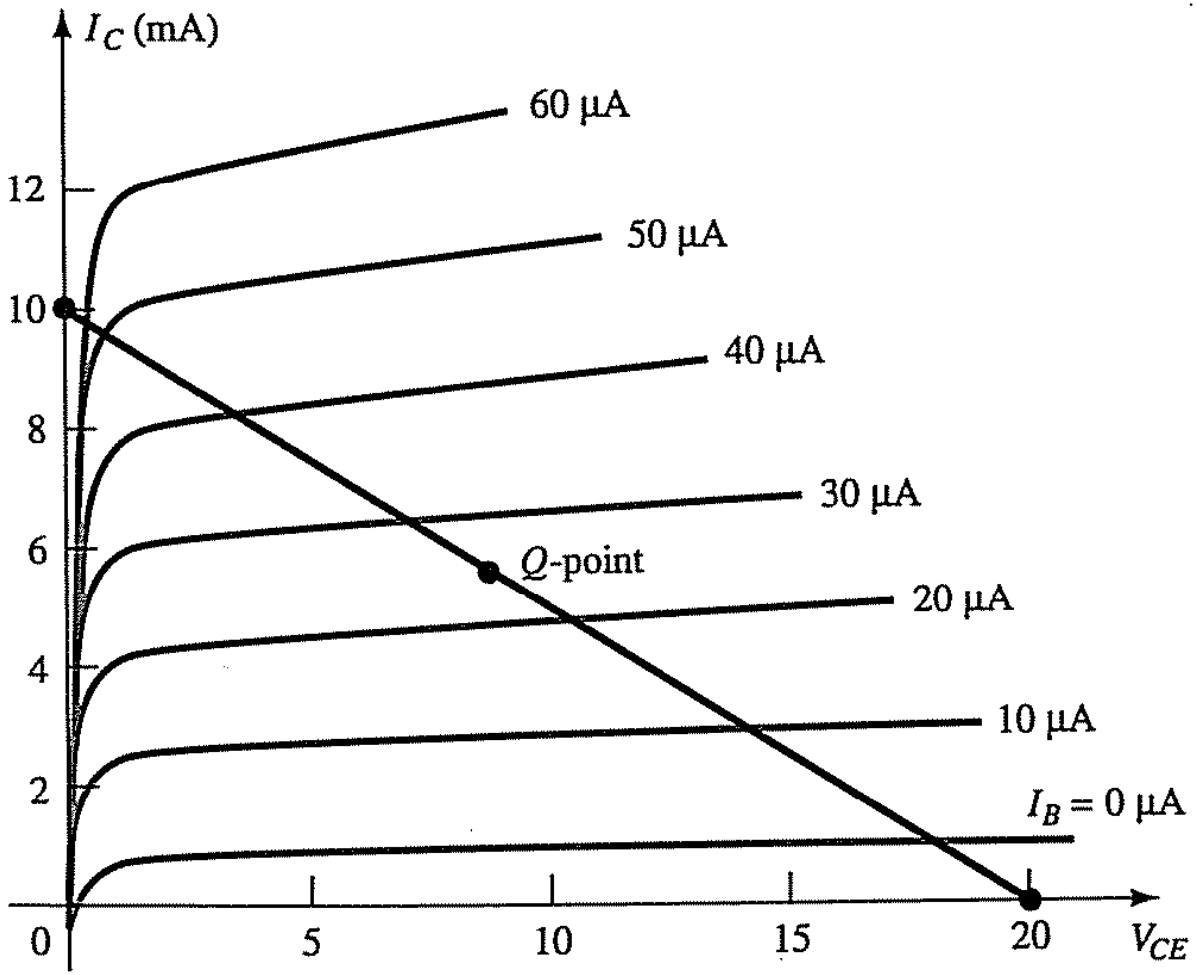
- The characteristic becomes:



Q-point is establish from I_B given

Example 4.3

- Given the load-line for fixed-bias configuration
- Determine V_{CC}, R_C and R_B



Example 4.3

- For $I_C = 0$:

$$V_{CE} = V_{CC} = 20$$

- For $V_{CE} = 0$:

$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{R_C} = 10m$$

$$\therefore R_C = 2\,\mathrm{k}\Omega$$

Example 4.3

- From the load-line given, Q-point is approximately at I_B = 25 μA
- For a fixed-bias configuration, I_B is defined by the equation:

$$I_B = \frac{V_{CC} - V_B}{R_B}$$

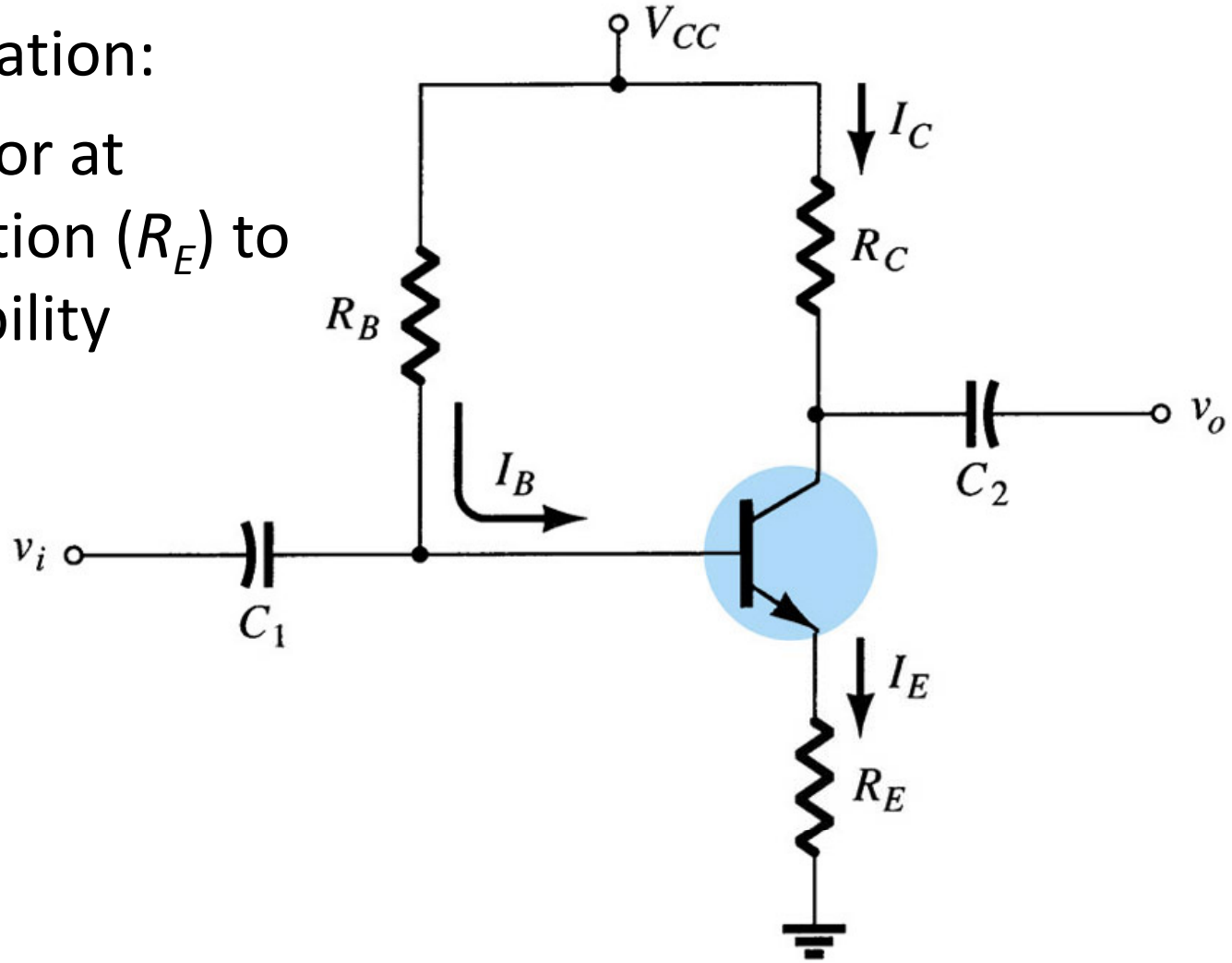
- Since that V_E = 0, resulting in $V_{BE} = V_B$ = 0.7, R_B can be calculated from the above equation:

$$25\mu = \frac{20 - 0.7}{R_B}$$

$$\therefore R_B = 772\,\text{k}\Omega$$

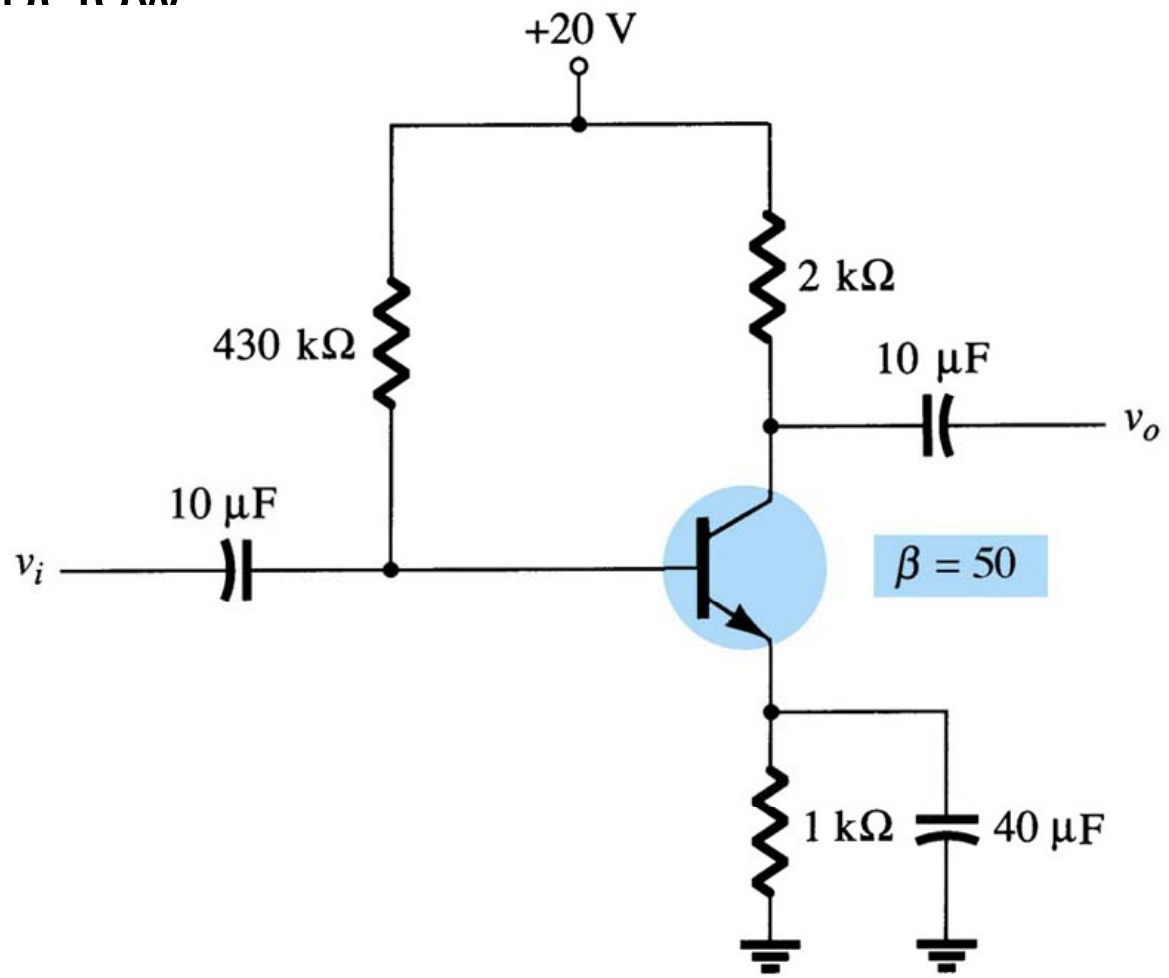
Emitter Bias Configuration

- The configuration:
- Added resistor at emitter junction (R_E) to improve stability



Example 4.4

- Determine I_B, I_C, V_{CE}, V_C, V_E, V_B & V_{BC} for the emitter bias circuit below:



Example 4.4

- Reference at B-E junction where V_{BE} = 0.7 V

$$V_{BE} = V_B - V_E = 0.7\ \text{V}$$

- Develop an equation for V_B:

$$I_B = \frac{V_{CC} - V_B}{R_B} = \frac{20 - V_B}{430k}$$

$$\therefore V_B = 20 - 430kI_B$$

- Then, develop an equation for V_E:

$$I_E = (\beta + 1)I_B = \frac{V_E}{R_E} = \frac{V_E}{1k} = 51I_B$$

$$\therefore V_E = 51kI_B$$

Example 4.4

- From V_B and V_E, insert to equation V_{BE}:

$$V_B - V_E = 0.7$$

$$20 - 430kI_B - 51kI_B = 0.7$$

$$\therefore I_B = 40.12\ \mu\text{A}$$

- For I_C: $I_C = \beta I_B = (50)(40.12\mu) = 2.01\,\text{mA}$

- Get V_C from I_C equation: $I_C = \dfrac{V_{CC} - V_C}{R_C}$

$$2.01m = \frac{20 - V_C}{2k} \qquad \therefore V_C = 15.98\,\text{V}$$

Example 4.4

- For the value of V_B, insert the value of I_B into the V_B equation:

$$V_B = 20 - 430kI_B = 20 - 430k(40.12\mu) = 2.75\ \text{V}$$

- For the value of V_E, insert the value of I_B into the V_E equation:

$$V_E = 51kI_B = 51k(40.12\mu) = 2.05\ \text{V}$$

- For V_{CE}:

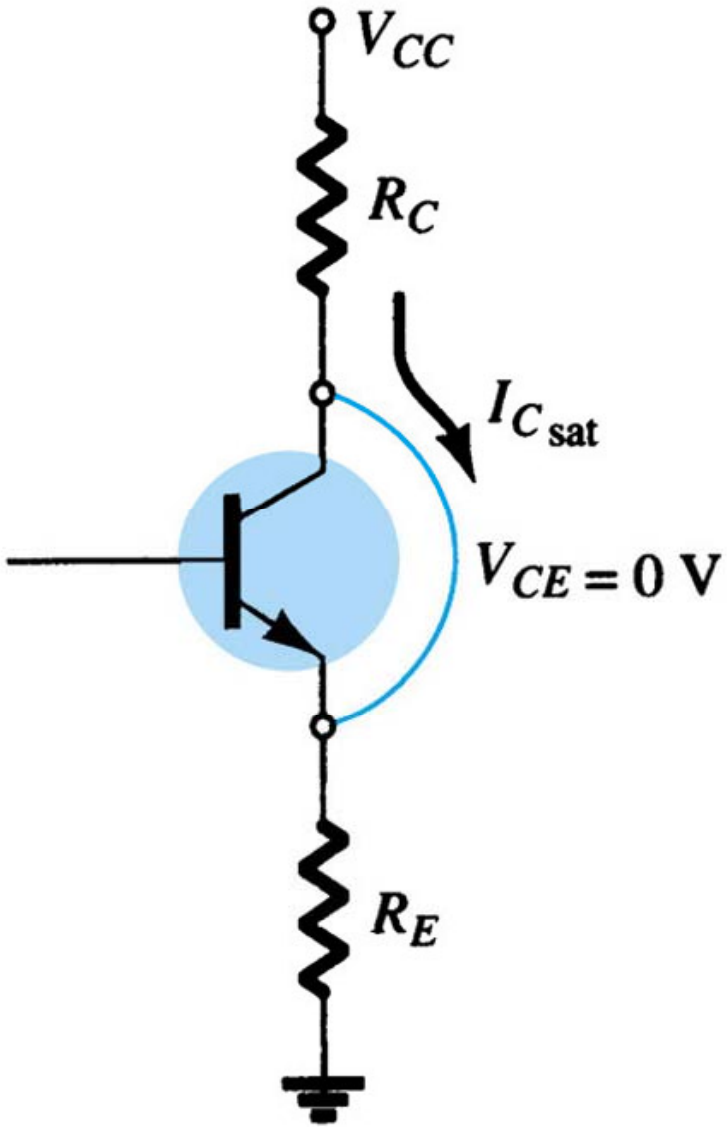
$$V_{CE} = V_C - V_E = 15.98 - 2.05 = 13.93\ \text{V}$$

- For V_{BC}:

$$V_{BC} = V_B - V_C = 2.75 - 15.98 = -13.23\ \text{V}$$

Saturation Level

- For the emitter-bias configuration, to determine the saturation current, $I_{C(sat)}$, the equivalent circuit is:



Saturation Level

- The calculation:

$$V_{CE} = 0 = V_C - V_E$$

$$\therefore V_C = V_E$$

- And: $I_C \approx I_E$
- For that, the saturation current becomes:

$$I_{C_{sat}} = \frac{V_{CC} - V_{CE} - 0}{R_C + R_E} = \frac{V_{CC} - 0 - 0}{R_C + R_E}$$

$$\therefore I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

Load-Line Analysis

- For V_{CE} = 0, the transistor will be in saturation region
- Taking the transistor saturation equation:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

- For I_C = 0:

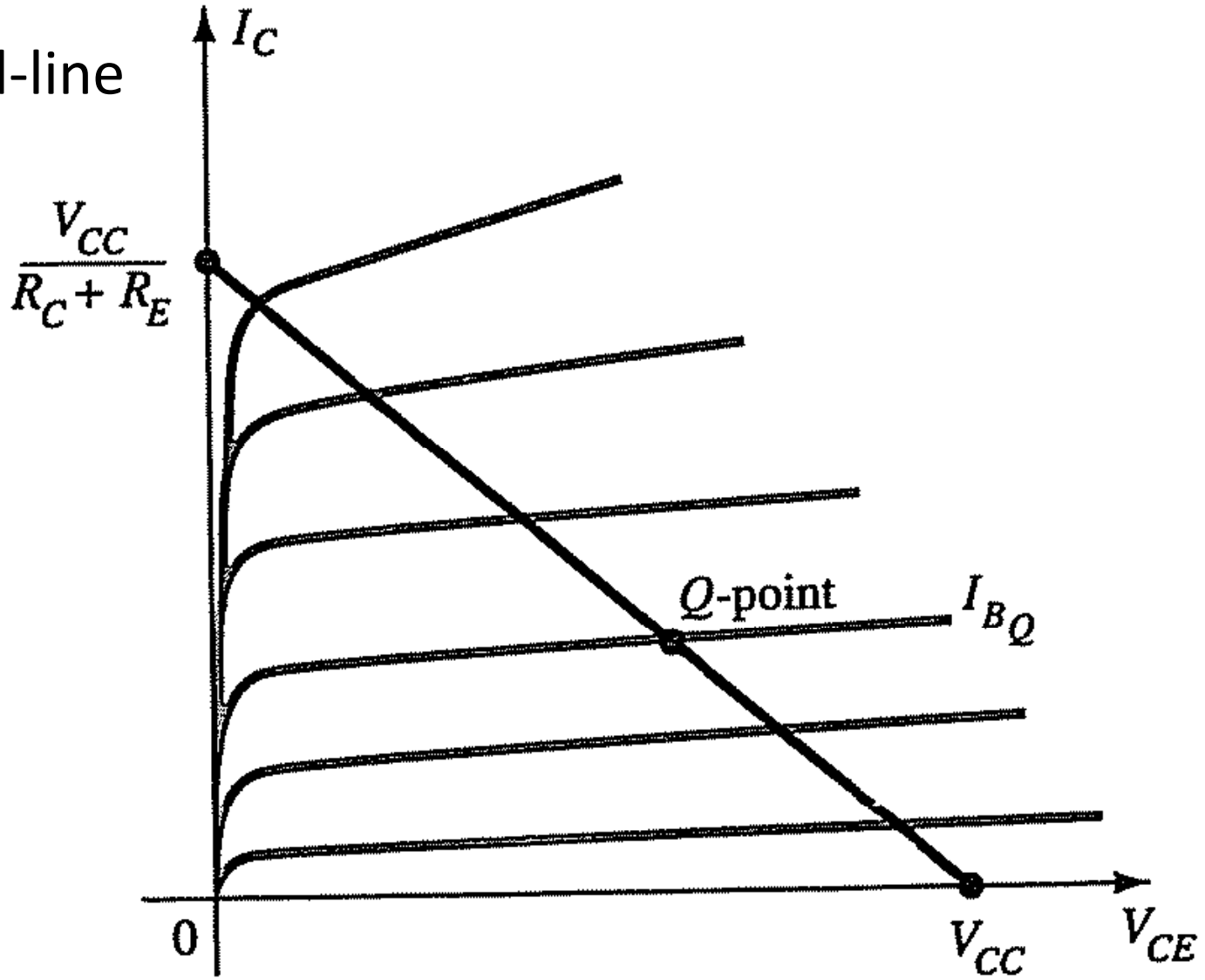
$$I_C \approx I_E$$

$$I_C = \frac{V_{CC} - V_{CE} - 0}{R_C + R_E} = 0$$

$$\therefore V_{CE} = V_{CC}$$

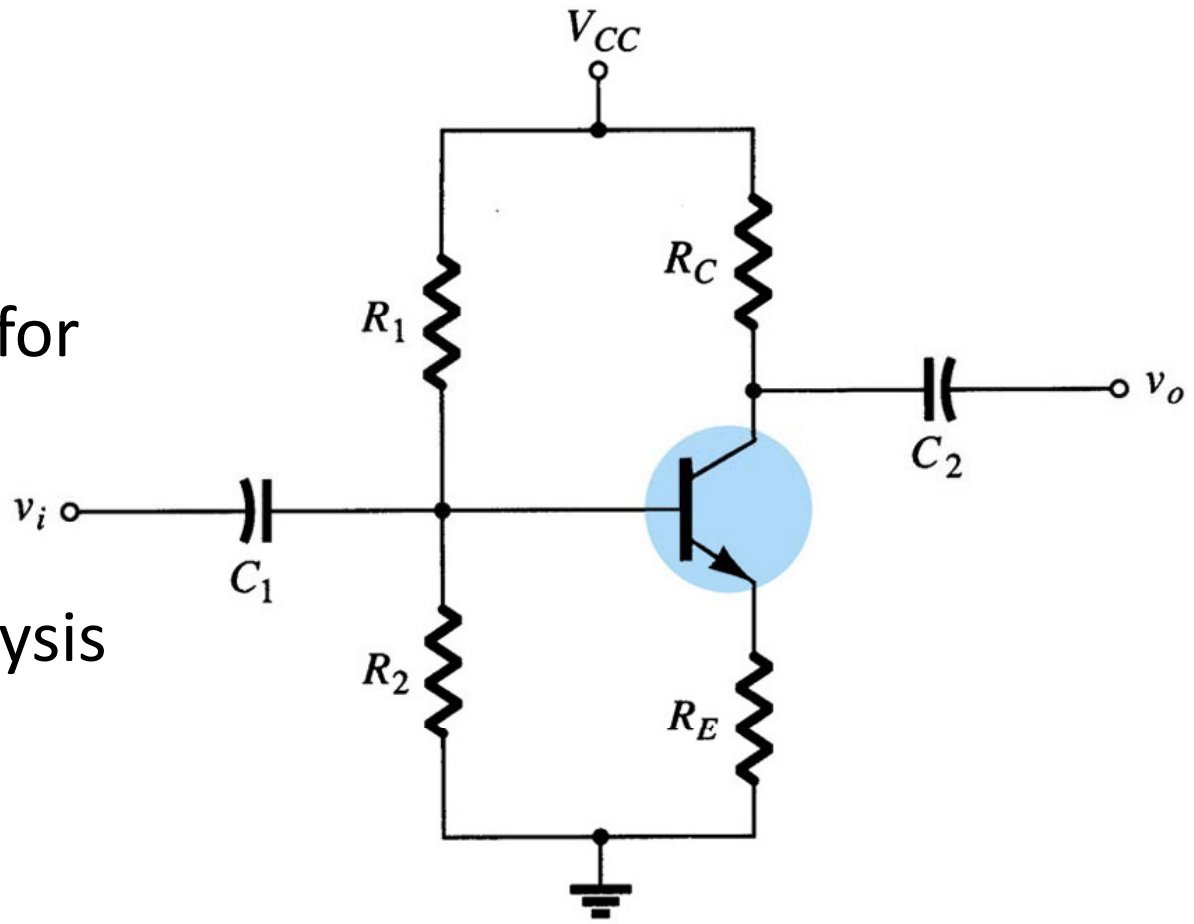
Load-Line Analysis

- So, the load-line becomes:



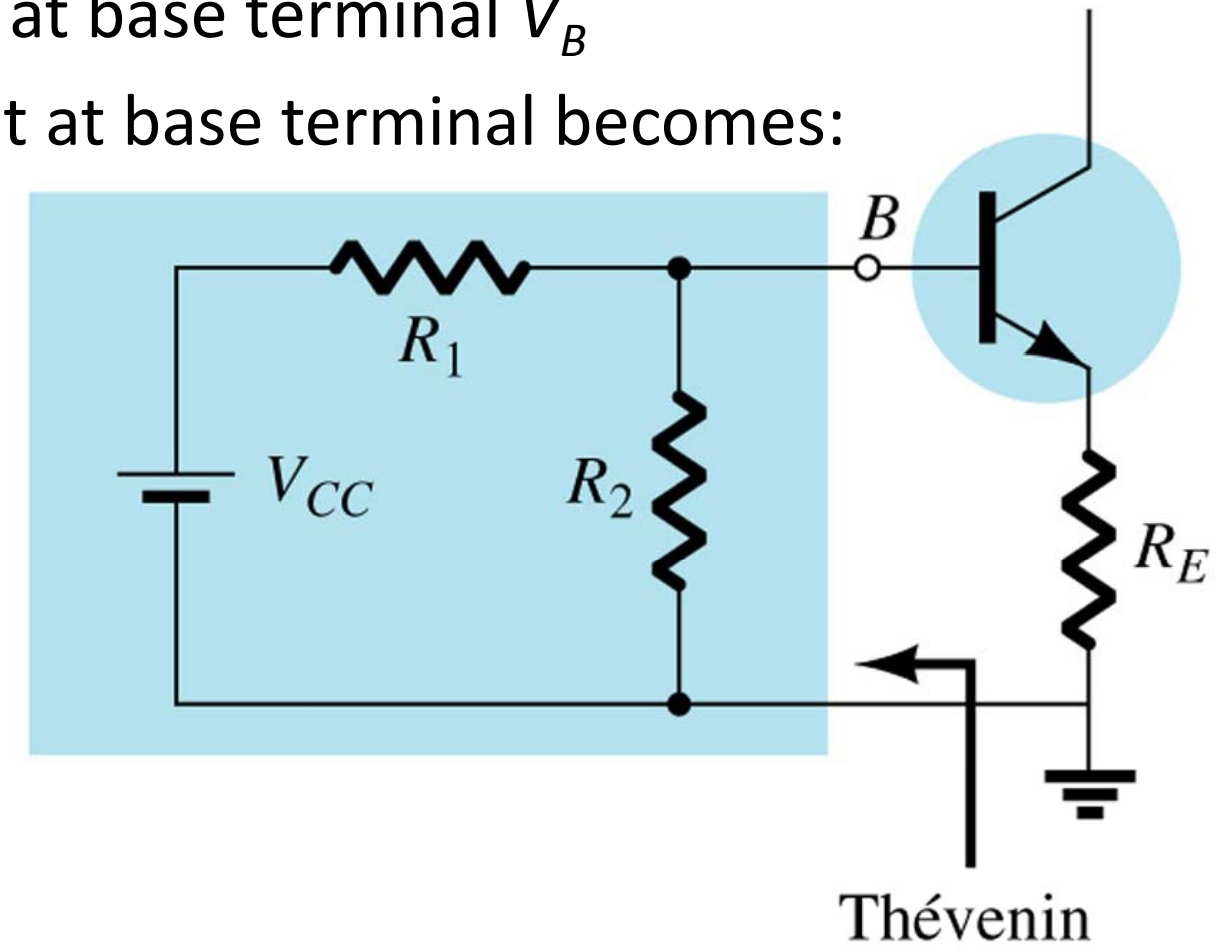
Voltage-Divider Bias Configuration

- The configuration:
- Added R_2 for R_B connected to ground
- Two kind of analysis for voltage-divider bias:
  - Exact Analysis
  - Approximate Analysis



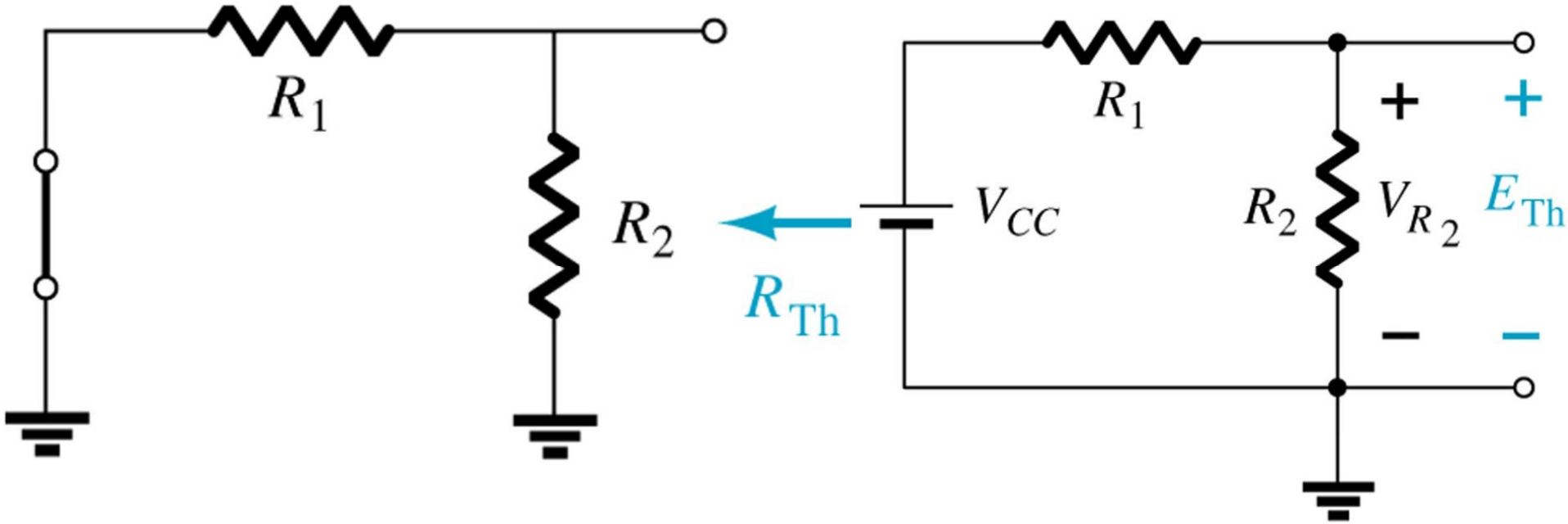
Exact Analysis

- Thevenin equivalent circuit is applied for V_{CC}, ground, R_1 and R_2 at base terminal V_B
- The circuit at base terminal becomes:



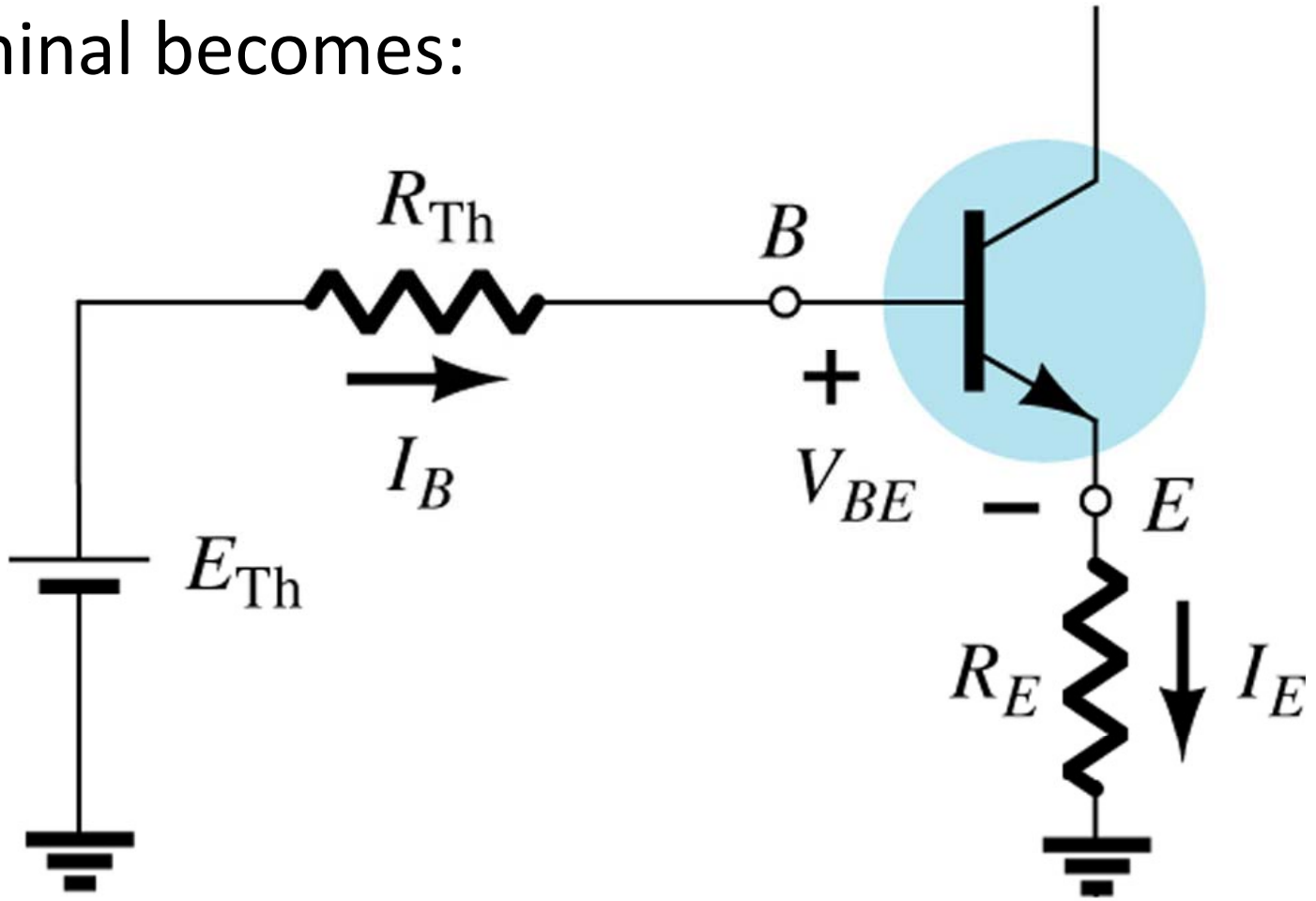
Exact Analysis

- R_{TH} and E_{TH} must be determined for Thevenin equivalent circuit
  - Determining R_{TH} - Determining E_{TH}



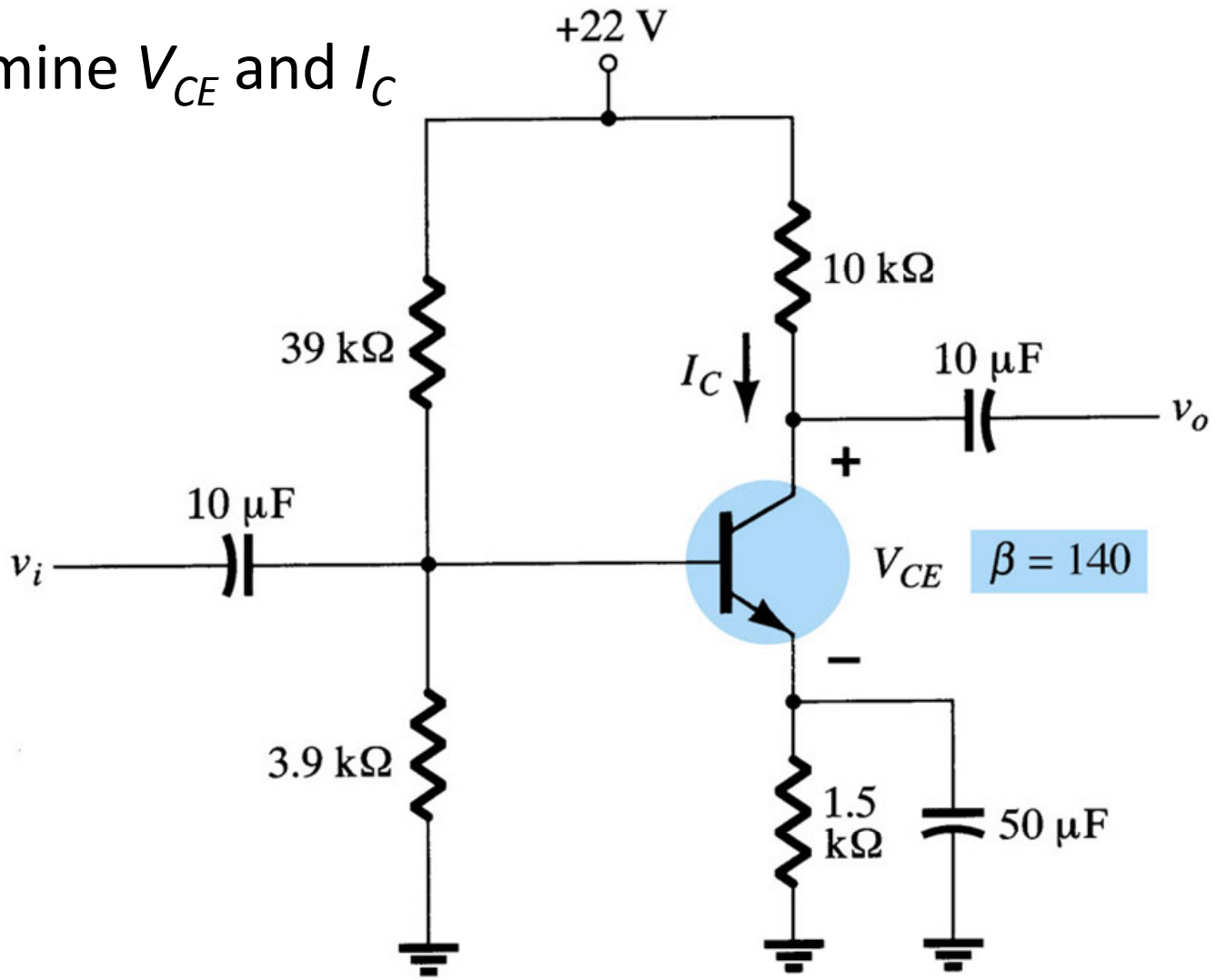
Exact Analysis

- The Thevenin equivalent circuit at base terminal becomes:



Example 4.7

- Determine V_{CE} and I_C



Example 4.7

- Determining R_{TH}:

$$R_{TH} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{(39k)(3.9k)}{39k + 3.9k} = 3.55\,\text{k}\Omega$$

- Determining E_{TH} (by applying nodal analysis at base terminal):

$$\frac{V_{CC} - E_{TH}}{R_1} = \frac{E_{TH}}{R_2}$$

$$\frac{22 - E_{TH}}{39k} = \frac{E_{TH}}{3.9k}$$

$$\therefore E_{TH} = 2\,\text{V}$$

Example 4.7

- Then applied the same technique as in fixed-bias or emitter-bias configuration to get the value of I_B:

$$V_{BE} = V_B - V_E = 0.7\ \text{V}$$

  - Reference at B-E junction where V_{BE} = 0.7 V
  - Develop an equation for V_B:

$$I_B = \frac{E_{TH} - V_B}{R_{TH}} = \frac{2 - V_B}{3.55k}$$

$$\therefore V_B = 2 - 3.55kI_B$$

  - Then, develop an equation for V_E:

$$I_E = (\beta + 1)I_B = \frac{V_E}{R_E} = \frac{V_E}{1.5k}$$

$$\therefore V_E = 211.5kI_B$$

Example 4.7

– From V_B and V_E, insert to equation V_{BE}:

$$V_{BE} = 0.7 = 2 - 3.55kI_B - 211.5kI_B$$

$$\therefore I_B = 6.05\ \mu\text{A}$$

– For I_C: $I_C = \beta I_B = (140)(6.05\mu) = 0.85\ \text{mA}$

– Get V_C from I_C equation:

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$0.85m = \frac{22 - V_C}{10k} \qquad \therefore V_C = 13.5\ \text{V}$$

Example 4.7

– For the value of V_E, insert the value of I_B into the V_E equation:

$$V_E = 211.5kI_B = 211.5k(6.05\mu) = 1.28\,\text{V}$$

– For V_{CE}:

$$V_{CE} = V_C - V_E = 13.5 - 1.28 = 12.22\,\text{V}$$

The Approximate Analysis

- For approximate analysis, we can assume:

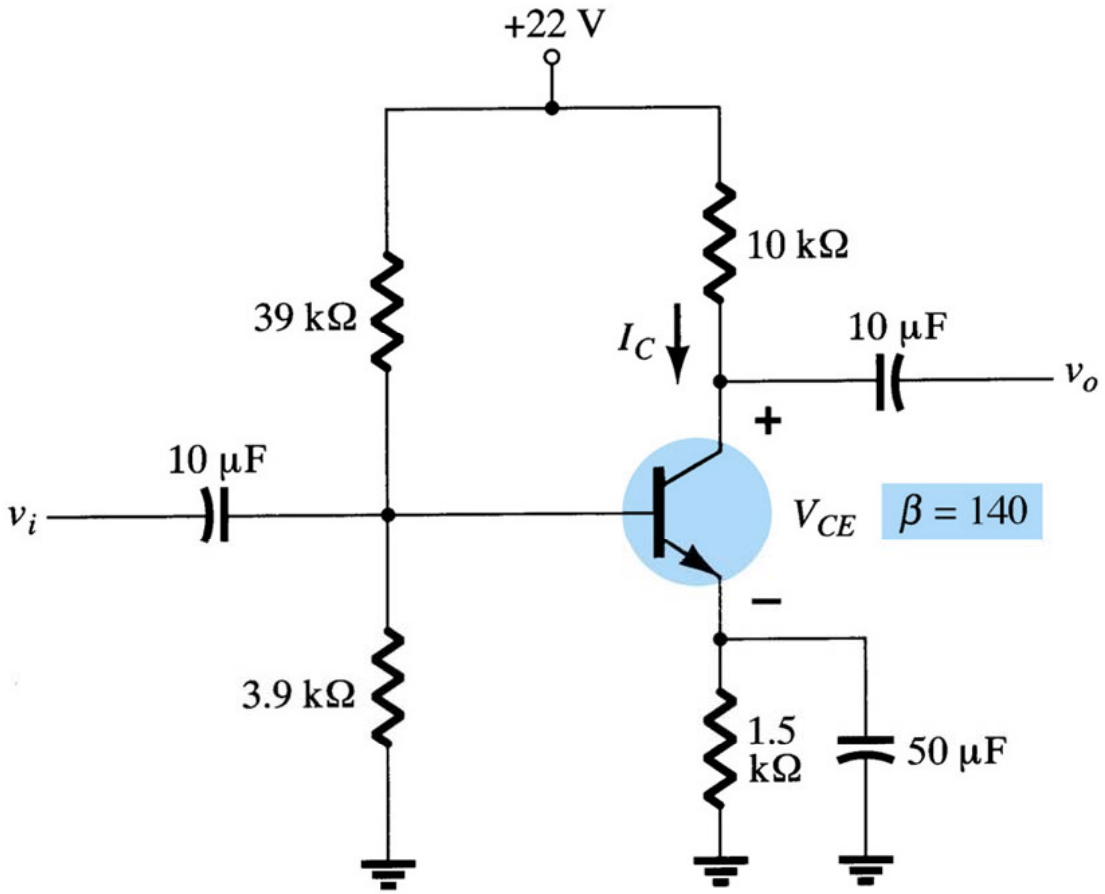
$$E_{TH} = V_B$$

- But the below condition must be satisfied so that the approximate analysis can be done:

$$\beta R_E \geq 10 R_2$$

Example 4.8

- Repeat Example 4.7 using the approximate analysis technique and compare the solutions for I_C and V_{CE}



Example 4.8

- Examine the condition for the approximate analysis technique:

$$\beta R_E = (140)(1.5k) = 210000$$

$$10R_2 = (10)(3.9k) = 39000$$

- So the equation $\beta R_E \geq 10R_2$ is satisfied resulting in $E_{TH} = V_B$
- By applying nodal analysis at node E_{TH}:

$$\frac{V_{CC} - V_B}{R_1} = \frac{V_B}{R_2}$$

$$\frac{22 - V_B}{39k} = \frac{V_B}{3.9k}$$

$$\therefore V_B = 2\ \text{V}$$

Example 4.8

- For V_E:

$$I_E = (\beta + 1) I_B = \frac{V_E}{R_E} = \frac{V_E}{1.5k}$$

$$\therefore V_E = 211.5k I_B$$

- From V_B and V_E, insert to equation V_{BE}:

$$V_{BE} = 0.7 = 2 - 211.5k I_B$$

$$\therefore I_B = 6.15\ \mu\text{A}$$

- For I_C:

$$I_C = \beta I_B = (140)(6.15\mu) = 0.86\ \text{mA}$$

Example 4.8

- For V_C:

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$0.86m = \frac{22 - V_C}{10k}$$

$$\therefore V_C = 13.4\,\text{V}$$

- For the value of V_E, insert the value of I_B into the V_E equation:

$$V_E = 211.5kI_B = 211.5k(6.15\mu) = 1.3\,\text{V}$$

- For V_{CE}: $V_{CE} = V_C - V_E = 13.4 - 1.3 = 12.1\,\text{V}$

Example 4.8

- By comparing the result from exact analysis with approximate analysis:

	I_C (mA)	V_{CE} (V)
Exact Analysis	0.85	12.22
Approximate Analysis	0.86	12.1

- The approximate value of I_c and V_{CE} is acceptable due to only small difference between them

Saturation Level

- The saturation level for the voltage-divider bias is the same as for the emitter bias configuration due to the existence of R_C and R_E

$$\therefore I_{C_{sat}} = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE} = 0}$$

Load Line Analysis

- As for the load-line analysis, the cutoff region still resulting in the same result as the fixed bias and emitter bias configuration:

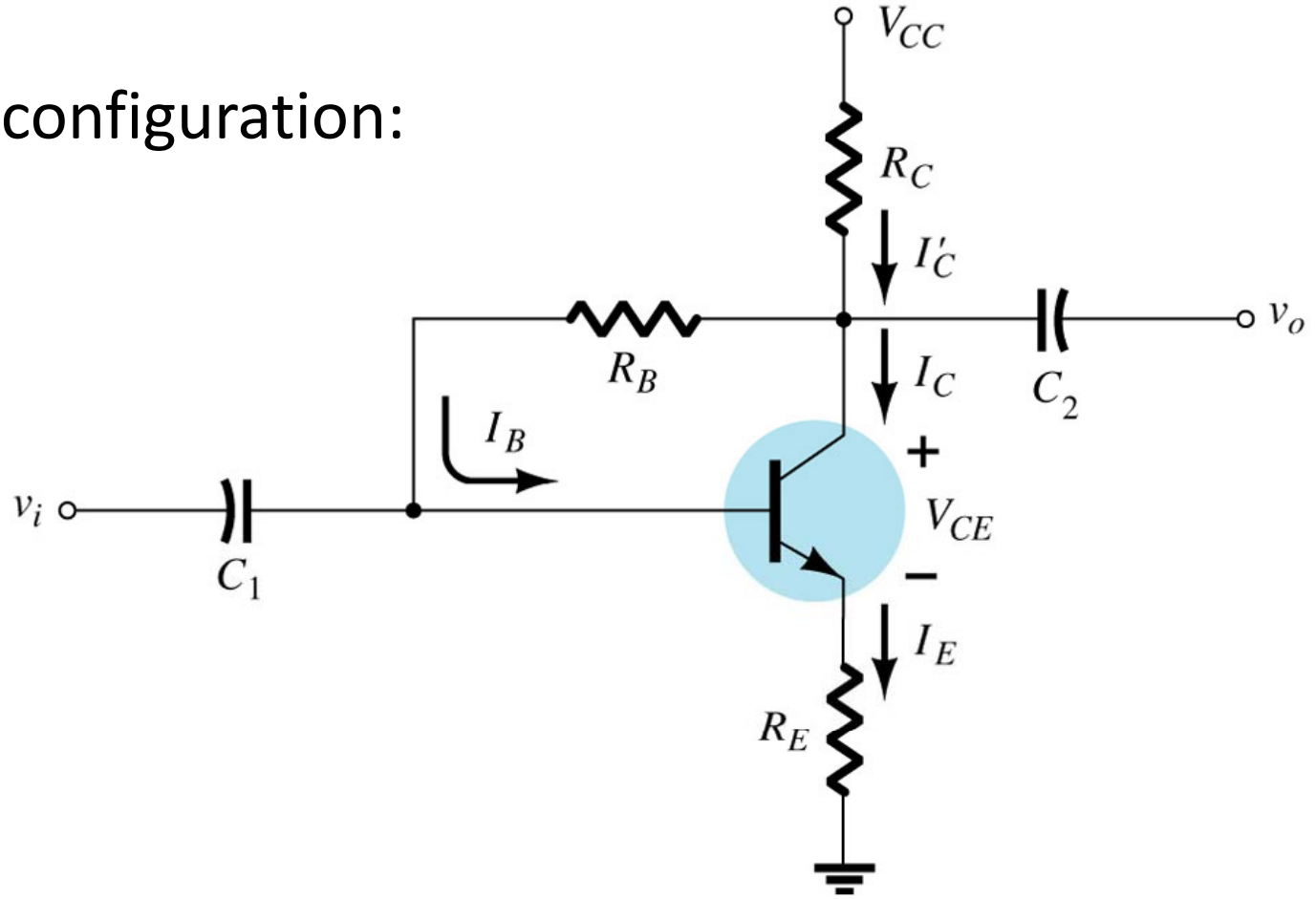
$$V_{CE} = V_{CC}\Big|_{I_C=0}$$

- And for the saturation region:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}\Bigg|_{V_{CE}=0}$$

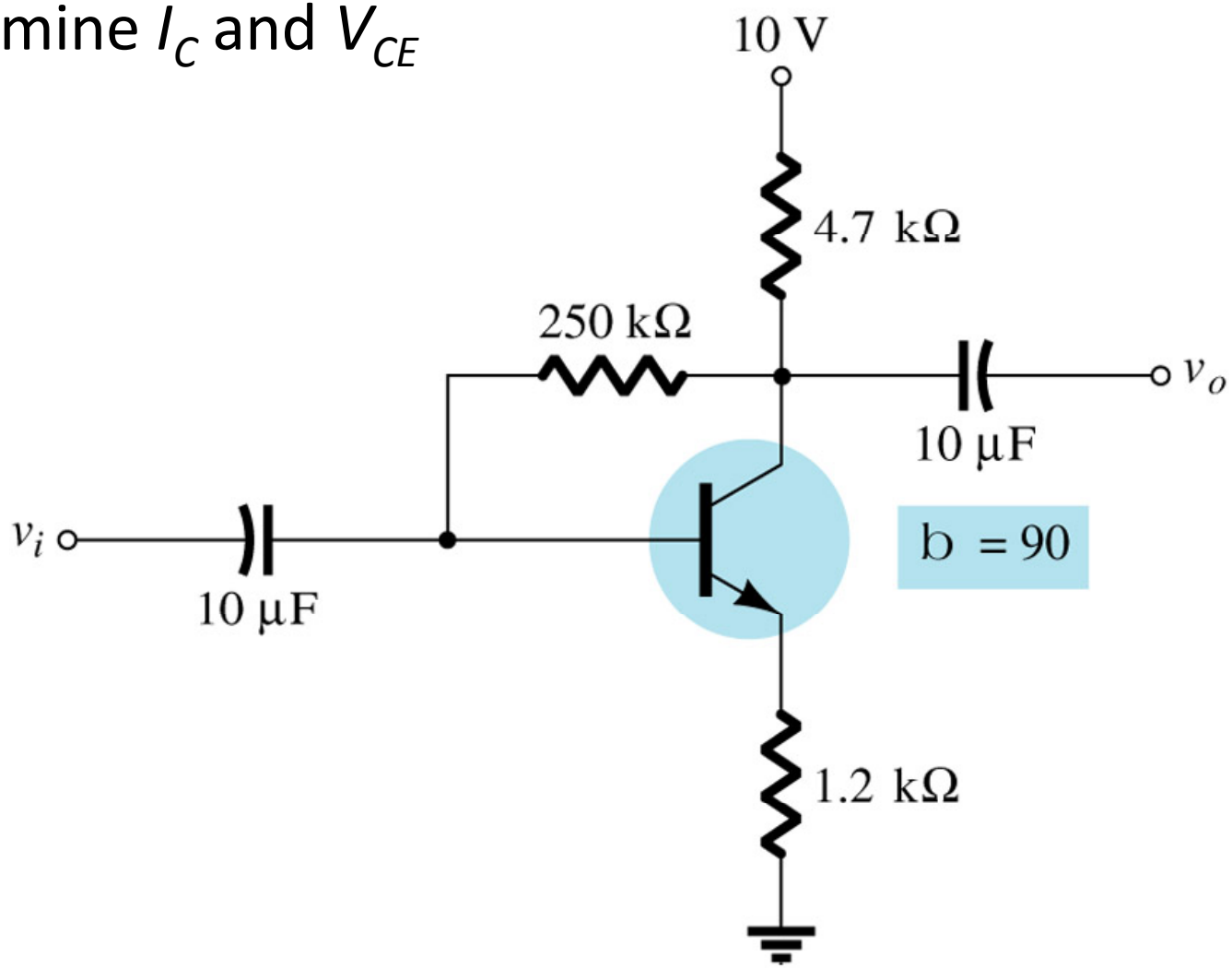
DC Bias with Voltage Feedback

- The base resistor (R_B) is connected to V_C instead of V_{CC}
- The configuration:



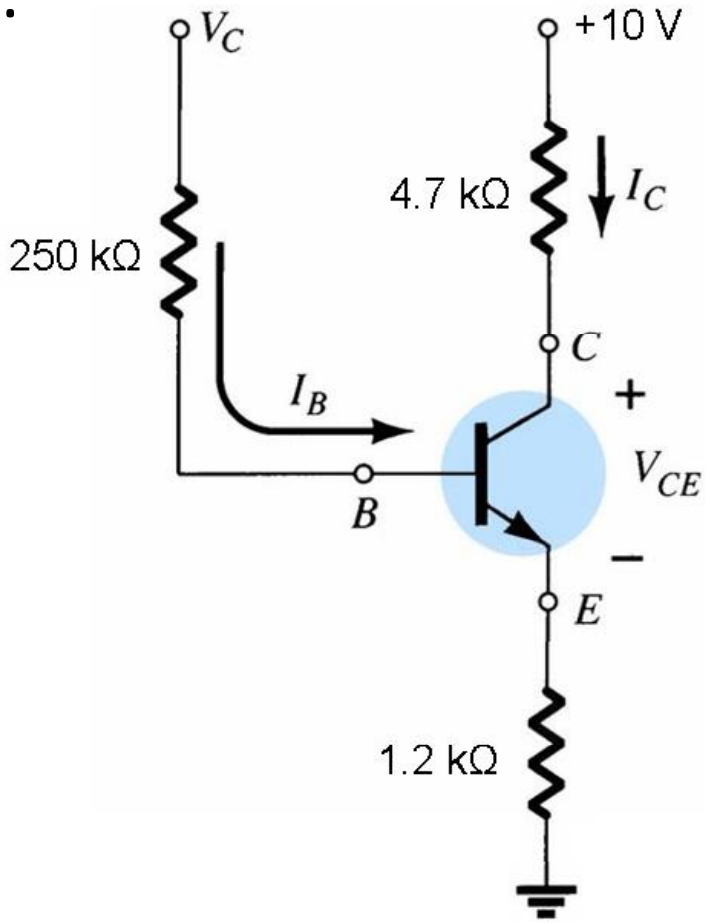
Example 4.11

- Determine I_C and V_{CE}



Example 4.11

- To make the analysis easier, the circuit is transformed into its equivalent circuit:



Example 4.11

- For V_B: $$I_B = \frac{V_C - V_B}{250k}$$
$$\therefore V_B = V_C - 250kI_B$$

- Because of the existence of V_C, the equation of V_C has to be obtained $$I_C = \beta I_B = \frac{10 - V_c}{4.7k}$$
$$\therefore V_C = 10 - 423kI_B$$

- Insert the V_C equation into the V_B equation:
$$V_B = 10 - 423kI_B - 250kI_B = 10 - 673kI_B$$

- For V_E: $$I_E = (\beta + 1)I_B = \frac{V_E}{1.2k}$$
$$\therefore V_E = 109.2kI_B$$

Example 4.11

- By substituting the V_{BE} equation:

$$V_{BE} = 0.7 = 10 - 673kI_B - 109.2kI_B$$

$$\therefore I_B = 11.89\ \mu\text{A}$$

- By applying the same technique as in other bias configuration that has been explained before to get I_C and V_{CE}:

$$I_C = 1.07\ \text{mA}$$

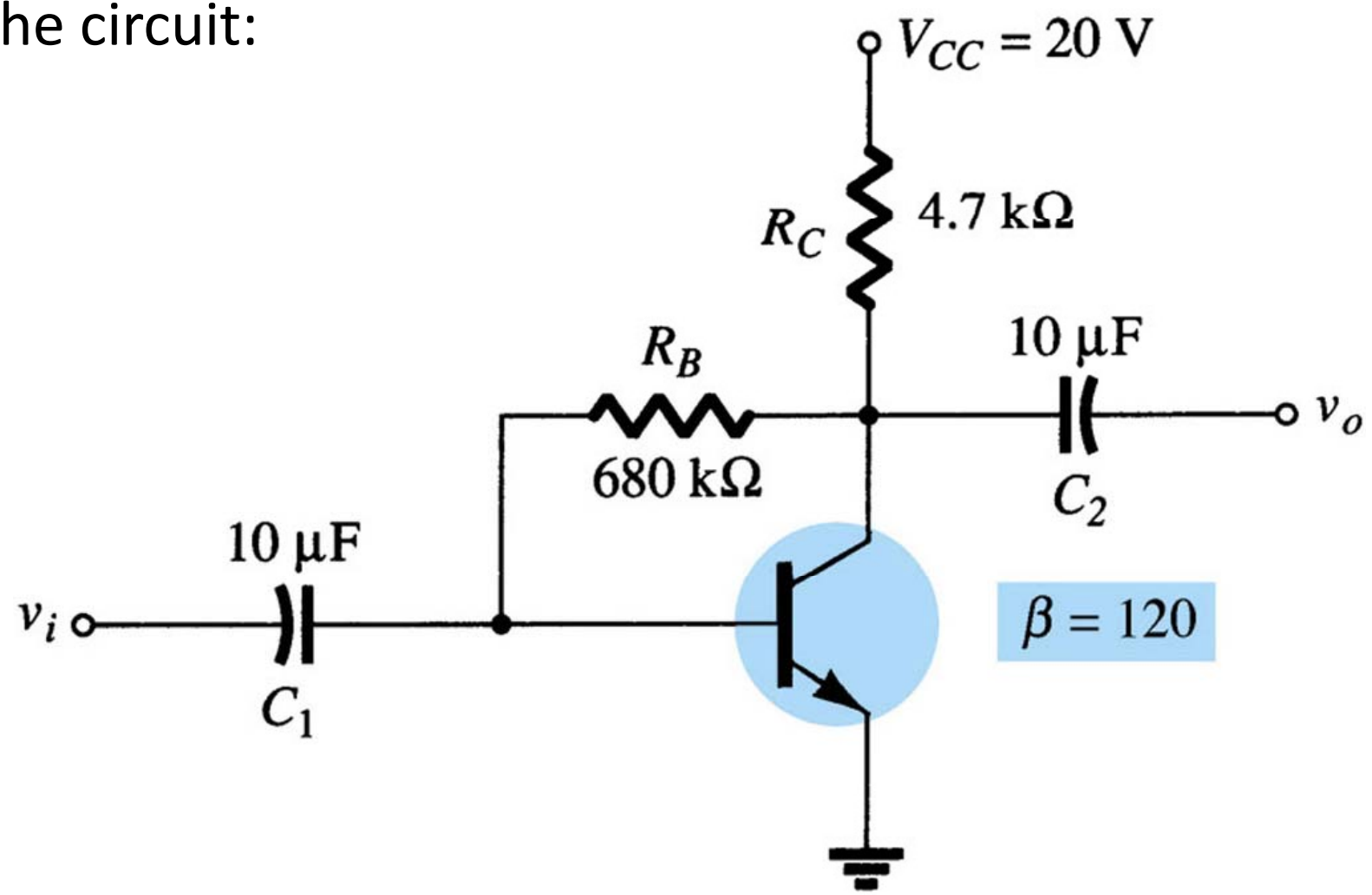
$$V_{CE} = 3.67\ \text{V}$$

Miscellaneous Bias Configurations

- There are many types of bias configuration other than the four that have been explained
- The calculation technique applied is the same for all BJT configuration, start with V_{BE} = 0.7 V because it is fixed for all *npn* transistor (V_{EB} = 0.7 V for *pnp* transistor)
- Once the base current (I_B) is obtained, all other current and voltage can be calculated
- In the examples provided in this subtopics, the calculation shown only to obtained I_B and all the other value can be calculated by applying the technique that have been explained before

Example 4.14

- The circuit:



Example 4.14

- The calculation:

$$I_C = \beta I_B = \frac{20 - V_C}{4.7k}$$

$$\therefore V_C = 20 - 564kI_B$$

$$I_B = \frac{V_C - V_B}{680k}$$

$$\therefore V_B = V_C - 680kI_B$$

$$V_B = 20 - 564kI_B - 680kI_B$$

$$\therefore V_B = 20 - 1244kI_B$$

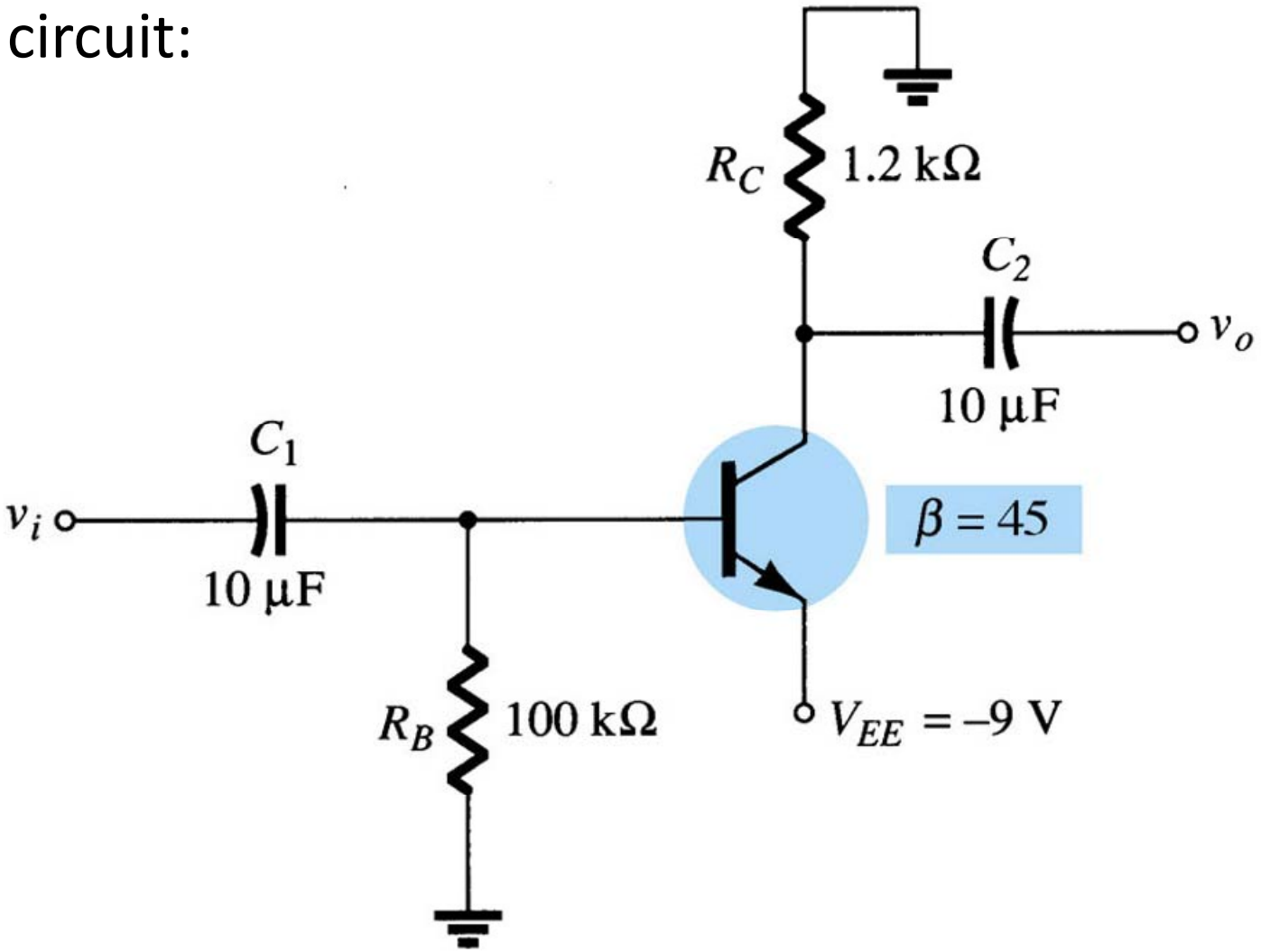
$$V_E = 0$$

$$V_{BE} = 0.7 = V_B - V_E = 20 - 1244kI_B - 0$$

$$\therefore I_B = 15.51\,\mu\text{A}$$

Example 4.15

- The circuit:



Example 4.15

- The calculation:

$$I_B = \frac{0 - V_B}{100k}$$

$$\therefore V_B = -100kI_B$$

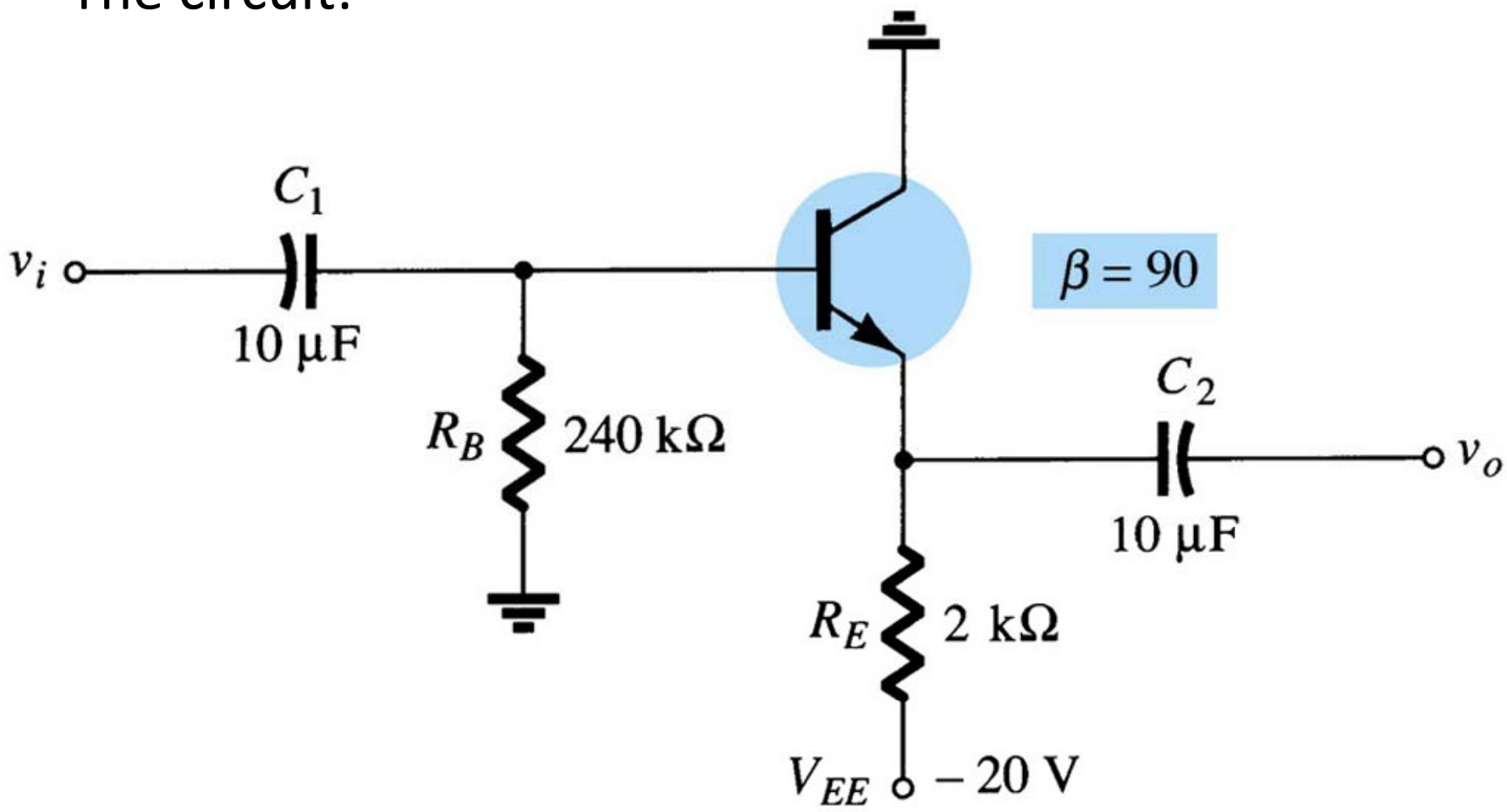
$$V_E = -9$$

$$V_{BE} = 0.7 = -100kI_B - (-9)$$

$$\therefore I_B = 83\ \mu\text{A}$$

Example 4.16

- The circuit:



Example 4.16

- The calculation:

$$I_B = \frac{0 - V_B}{240k}$$

$$\therefore V_B = -240kI_B$$

$$I_E = (\beta + 1)I_B = \frac{V_E - (-20)}{2k}$$

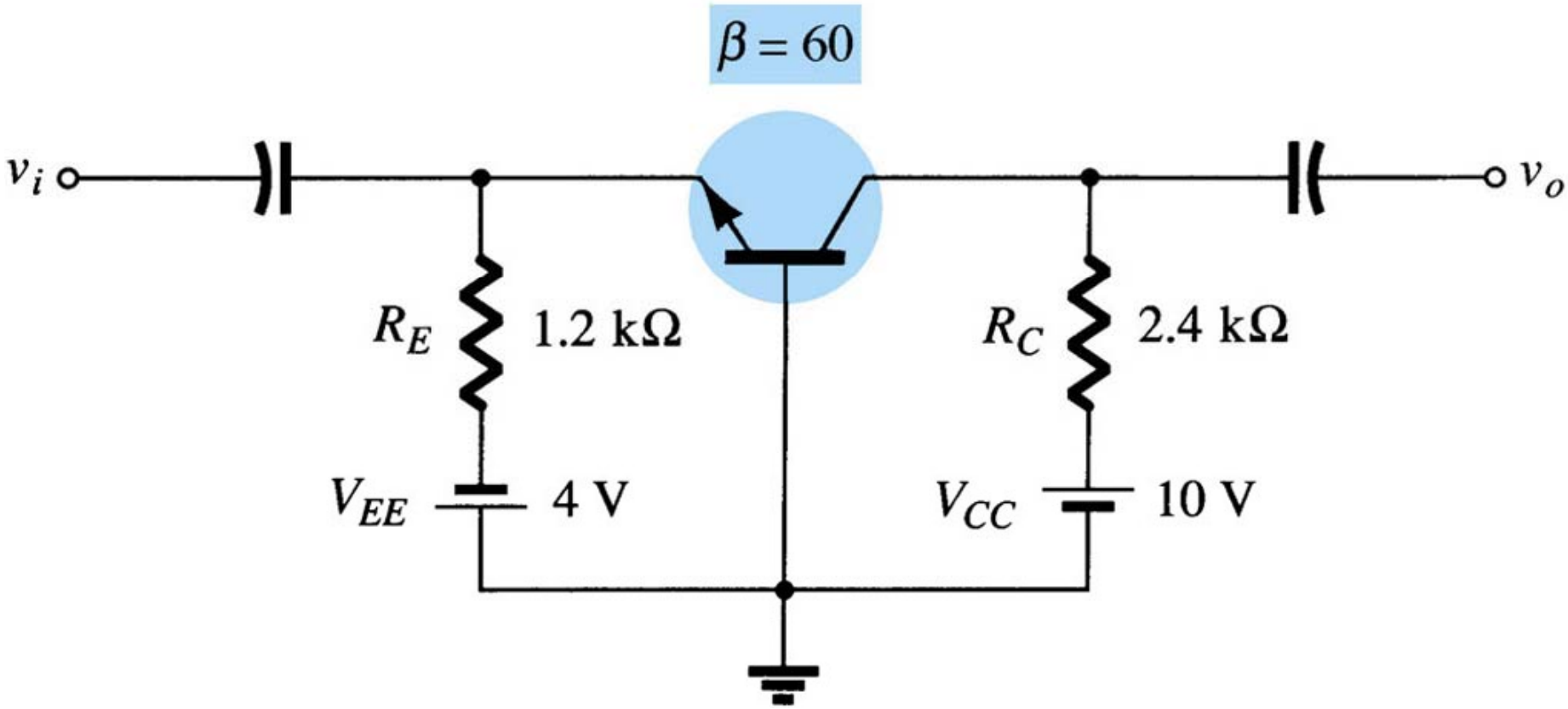
$$\therefore V_E = 182kI_B - 20$$

$$V_{BE} = 0.7 = V_B - V_E = -240kI_B - \left(182kI_B - 20\right)$$

$$\therefore I_B = 45.73\ \mu\text{A}$$

Example 4.17

- The circuit:



Example 4.17

- The calculation:

$$V_B = 0$$

$$I_E = (\beta + 1) I_B = \frac{V_E - (-4)}{1.2k}$$

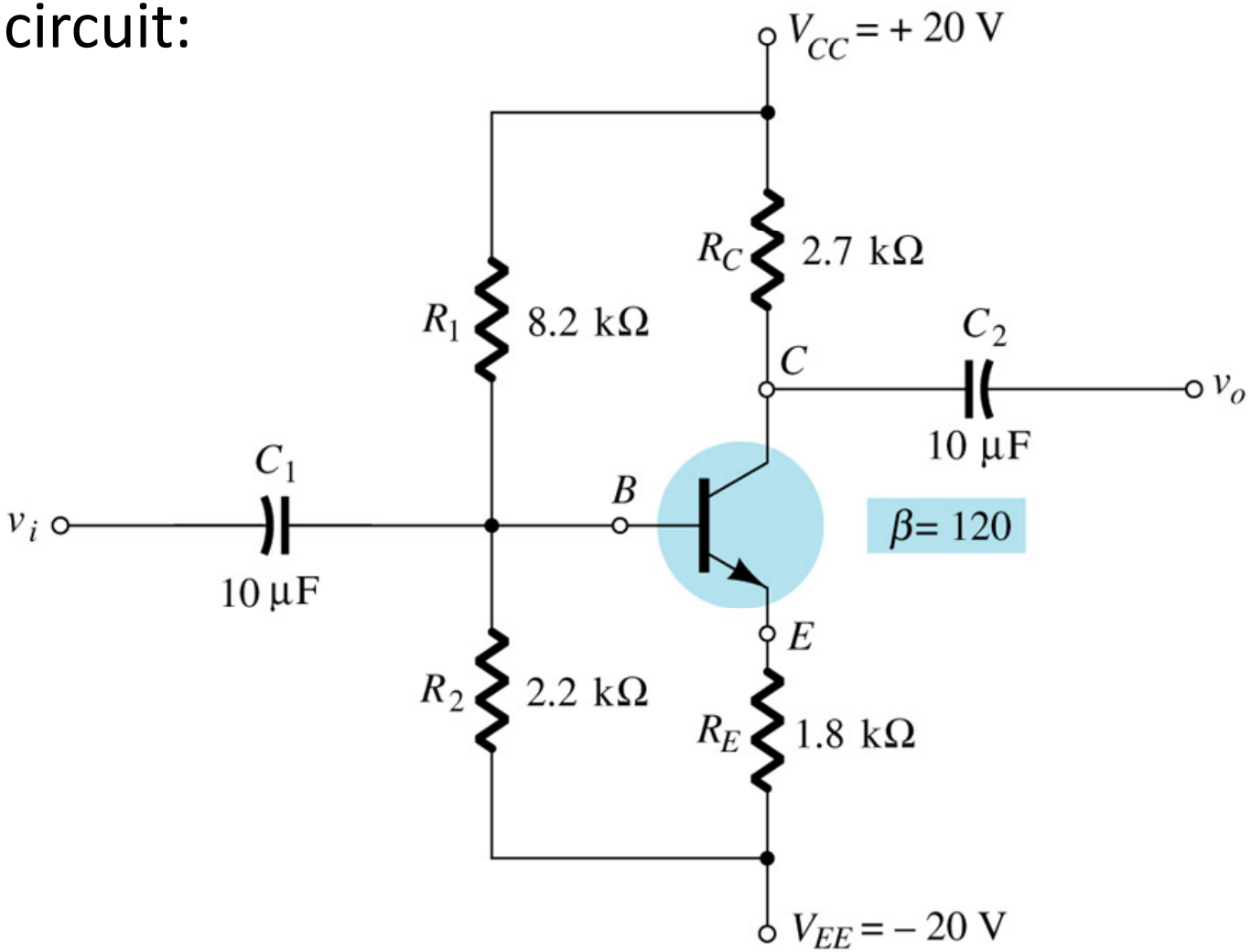
$$\therefore V_E = 73.2 k I_B - 4$$

$$V_{BE} = 0.7 = 0 - \left(73.2 k I_B - 4\right)$$

$$\therefore I_B = 45.08\ \mu\text{A}$$

Example 4.18

- The circuit:



Example 4.18

- The calculation:

$$R_{TH} = \frac{(8.2k)(2.2k)}{8.2k + 2.2k} = 1.73\,\text{k}\Omega$$

$$\frac{20 - E_{TH}}{8.2k} = \frac{E_{TH} - (-20)}{2.2k}$$

$$\therefore E_{TH} = -11.54\,\text{V}$$

$$I_E = (\beta + 1) I_B = \frac{V_E - (-20)}{1.8k}$$

$$\therefore V_E = 217.8k I_B - 20$$

$$I_B = \frac{E_{TH} - V_B}{R_{TH}} = \frac{-11.54 - V_B}{1.73k}$$

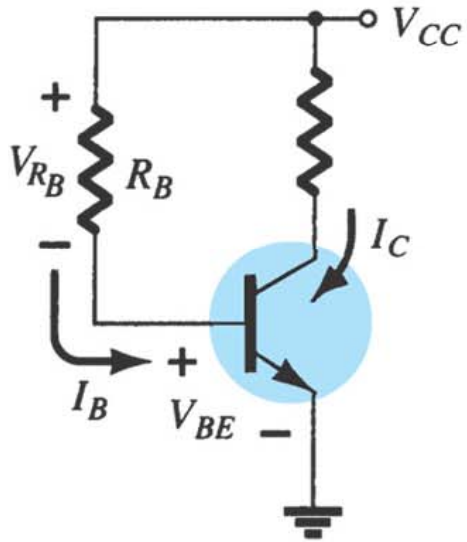
$$\therefore V_B = -11.54 - 1.73k I_B$$

$$V_{BE} = 0.7$$

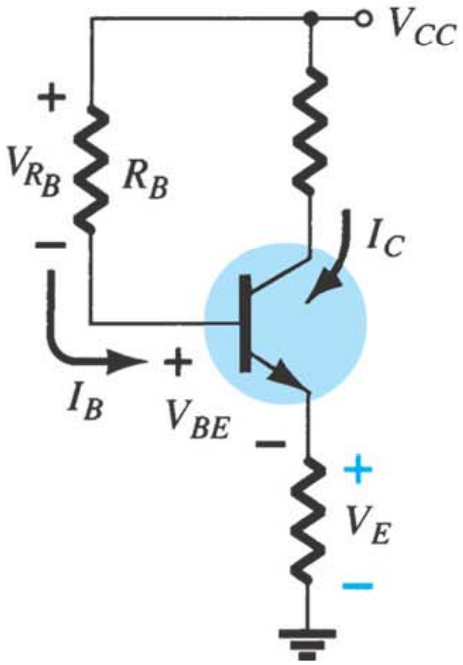
$$= -11.54 - 1.73k I_B - \left(217.8k I_B - 20\right)$$

$$\therefore I_B = 35.35\,\mu\text{A}$$

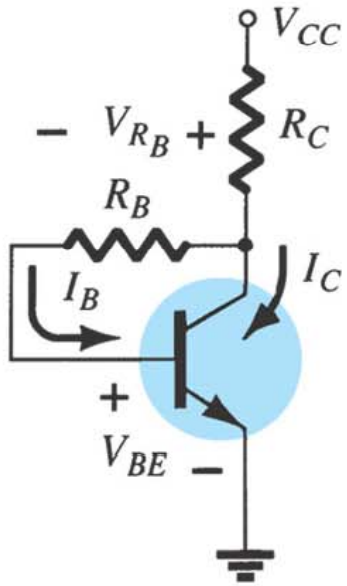
Bias Stabilization



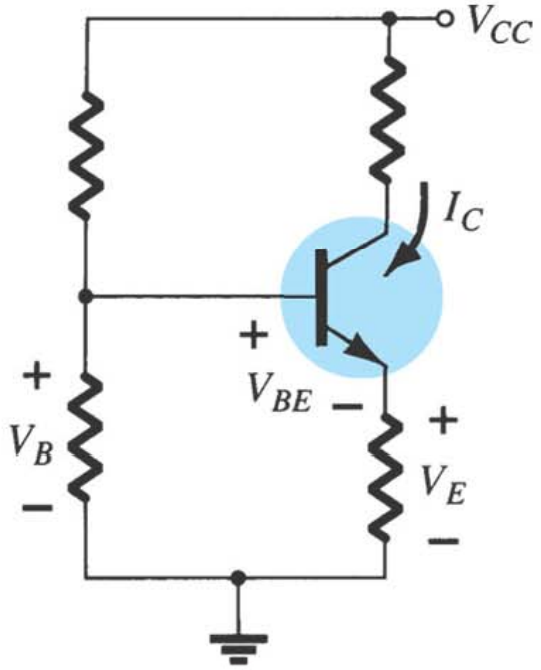
Fixed-bias
– β dependent
– not stable



Emitter-bias
– stabilization increase
– still β dependent



DC bias with voltage feedback
– stabilization increase due to feedback of R_B
– less β dependent



Voltage-divider bias
– β independent
– stabilize

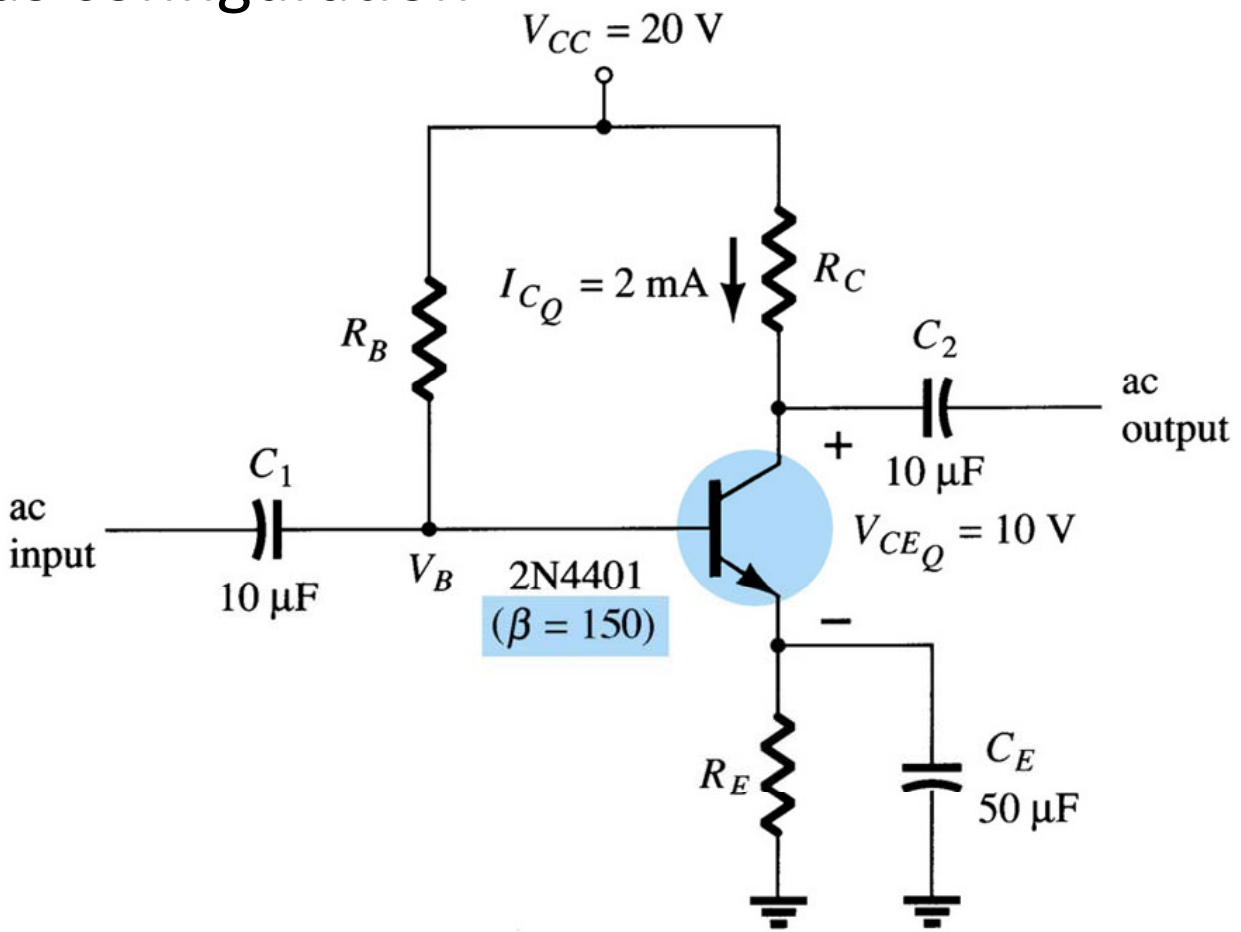
Design Operation

- All the technique that has been explained previously in this topic are used for circuit analysis where the current and voltage are calculated and obtained
- In design operation, some of the current and voltage are given meanwhile the value of the resistors have to be obtained in order to design the required bias configuration (all the techniques still applied)
- Only 1 assumption has to be made in design operation that is:

$$V_E = \frac{1}{10} V_{CC}$$

Example 4.22

- Determine the all resistors value in designing a emitter-bias configuration



Example 4.22

- According to the design operation assumption:

$$V_E = \frac{1}{10} V_{CC} = \frac{1}{10}(20) = 2\,\text{V}$$

- From the V_{CE} value given:

$$V_{CE} = 10 = V_C - V_E = V_C - 2$$
$$\therefore V_C = 12\,\text{V}$$

- To obtain R_C:

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$2m = \frac{20 - 12}{R_C}$$

$$\therefore R_C = 4\,\text{k}\Omega$$

Example 4.22

- Due to $I_C \approx I_E$, R_E is obtained: $I_E = \dfrac{V_E}{R_E}$

$$2m = \frac{2}{R_E}$$

$$\therefore R_E = 1\,\text{k}\Omega$$

- Due to IC = (β+1)IB, RB is obtained:

$$V_{BE} = 0.7 = V_B - V_E$$

$$0.7 = V_B - 2$$

$$\therefore V_B = 2.7\,\text{V}$$

$$I_C = (\beta + 1) I_B$$

$$2m = 151 I_B$$

$$\therefore I_B = 13.24\,\mu\text{A}$$

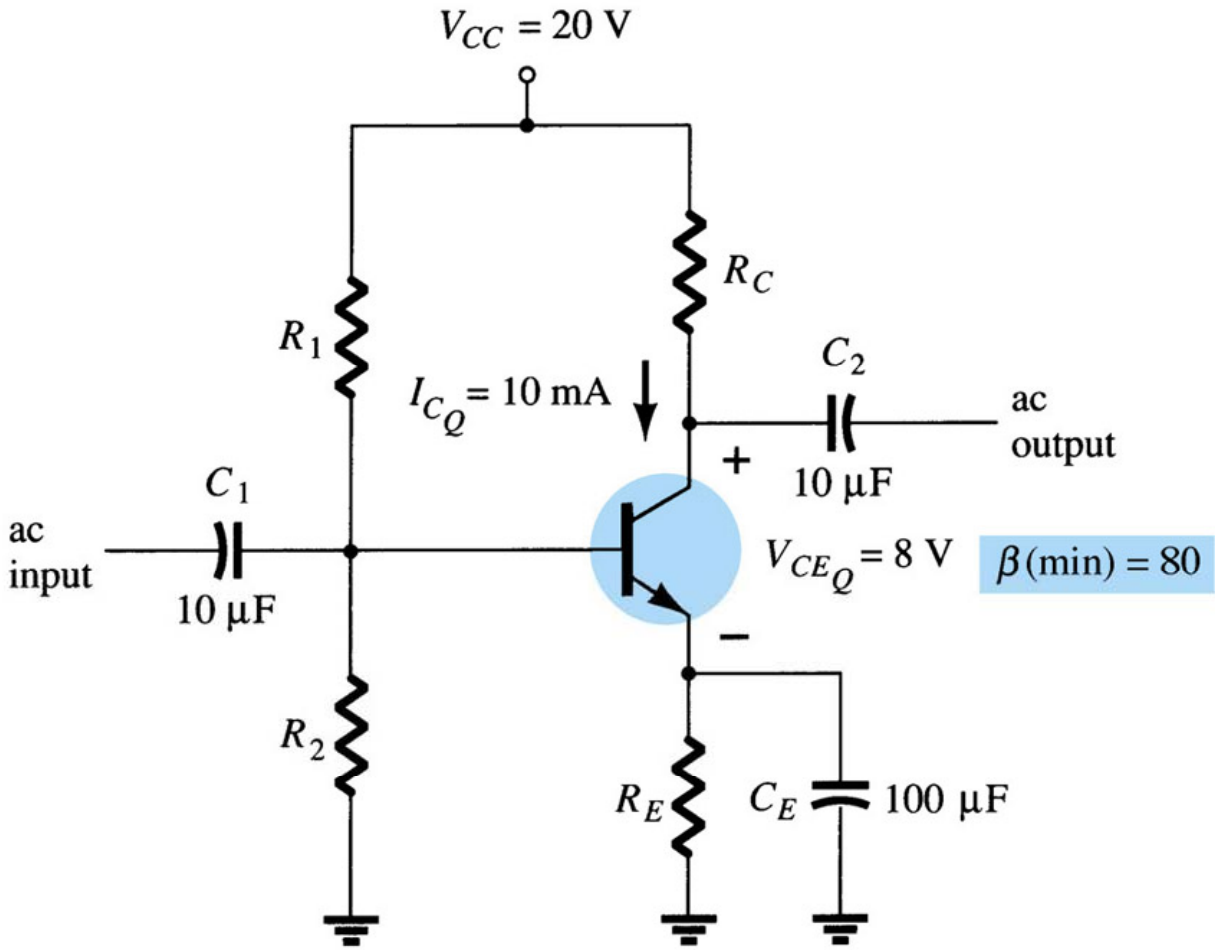
$$I_B = \frac{V_{CC} - V_B}{R_B}$$

$$13.24\mu = \frac{20 - 2.7}{R_B}$$

$$\therefore R_B = 1.31\,\text{M}\Omega$$

Example 4.23

- Determine the all resistors value in designing a voltage-divider bias configuration



Example 4.23

- According to the design operation assumption:

$$V_E = \frac{1}{10} V_{CC} = \frac{1}{10}(20) = 2\ \text{V}$$

- From the V_{CE} value given:

$$V_{CE} = 8 = V_C - V_E = V_C - 2$$

$$\therefore V_C = 10\ \text{V}$$

- To obtain R_C:

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$10m = \frac{20 - 10}{R_C}$$

$$\therefore R_C = 1\ \text{k}\Omega$$

Example 4.22

- Due to $I_C \approx I_E$, R_E is obtained:

$$I_E = \frac{V_E}{R_E}$$

$$10m = \frac{2}{R_E}$$

$$\therefore R_E = 200\,\Omega$$

- To ease the calculation, approximate analysis is used so that R_{TH} are ignored: $\beta R_E \geq 10R_2$
- For minimum β:

$$\beta R_E = 10R_2$$

$$(80)(200) = 10R_2$$

$$\therefore R_2 = 1.6\,\text{k}\Omega$$

$$V_{BE} = 0.7 = V_B - V_E$$

$$0.7 = V_B - 2$$

$$\therefore V_B = 2.7\,\text{V}$$

Example 4.22

- Applying nodal analysis at node V_B to obtain the value of R_1:

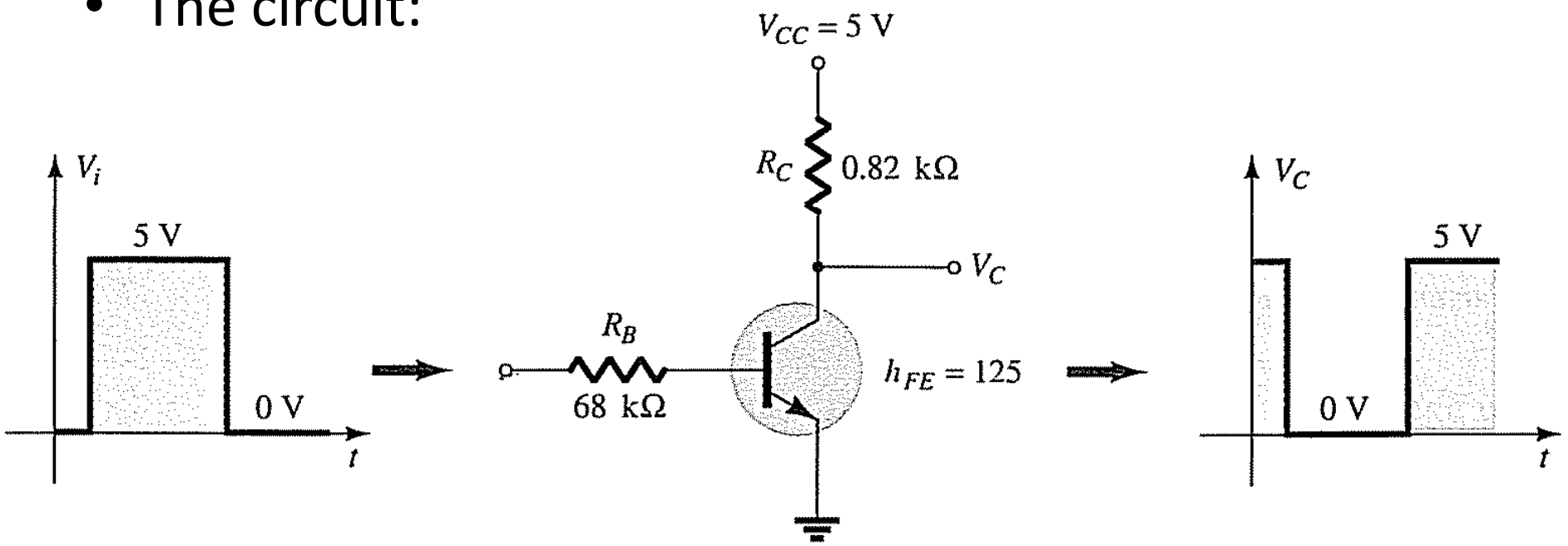
$$\frac{20-2.7}{R_1}=\frac{2.7}{1.6k}$$

$$\therefore R_1 = 10.25\,\text{k}\Omega\,(\text{use}\,10\,\text{k}\Omega)$$

- Note that the value obtained is recommended using 10 kΩ due to 10.25 kΩ is not exist in the real world

Transistor Switching Networks

- Transistor also can be used as switches for computer applications
- One of the example in computer application is the transistor usage as an inverter
- The circuit:



Transistor Switching Networks

- Examine the circuit to obtained the load-line analysis point at cutoff and saturation region

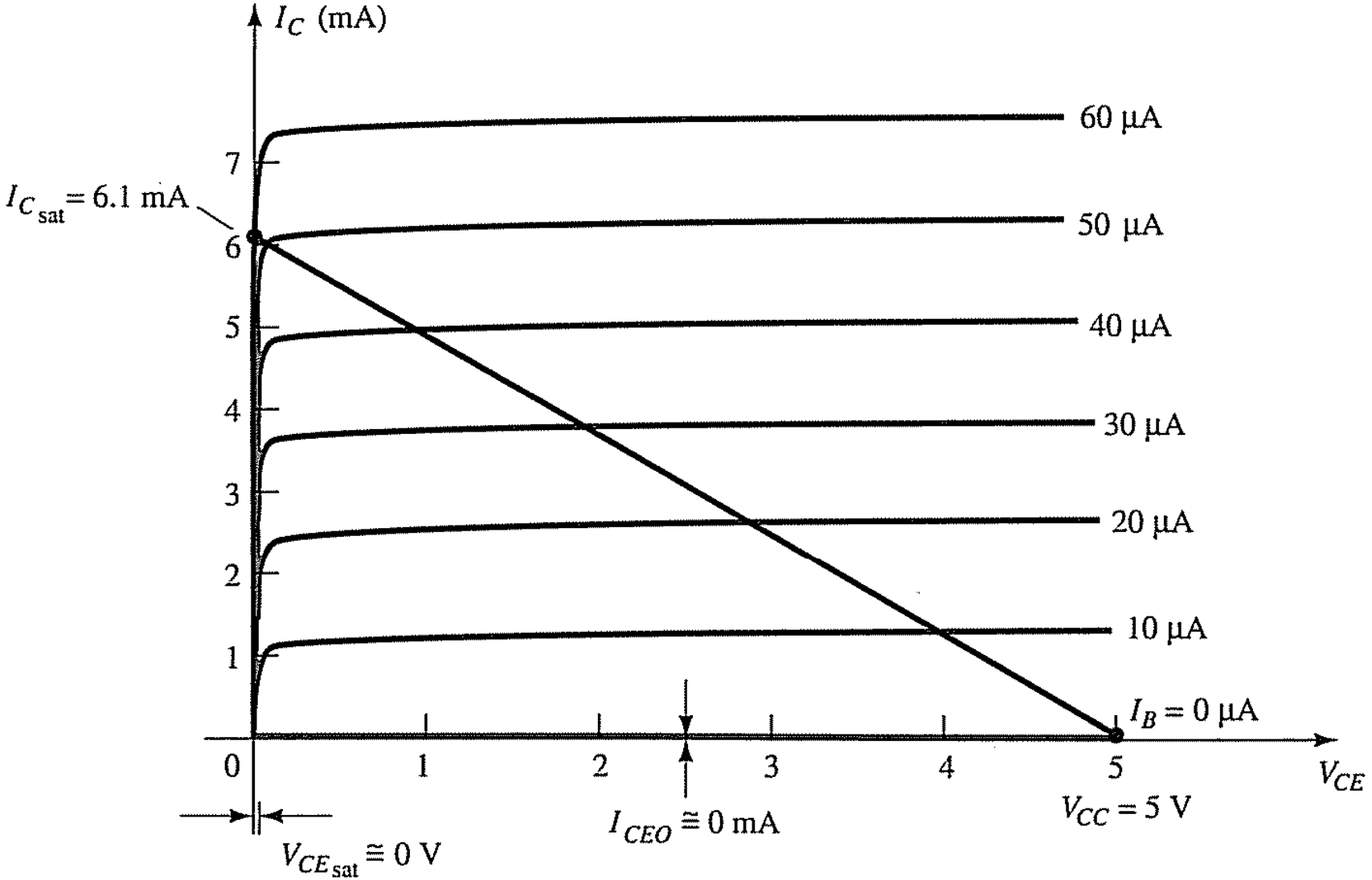
$$V_{CE} = V_{CC} = 5\ \text{V}\Big|_{I_C=0}\ (\text{cutoff - region})$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5}{0.82k} = 6.1\,\text{mA}\ (\text{saturation region})$$

- The transistor will work in the cutoff region and saturation region, as for that 2 Q-point will be achieved

Transistor Switching Networks

- The load-line analysis will become:

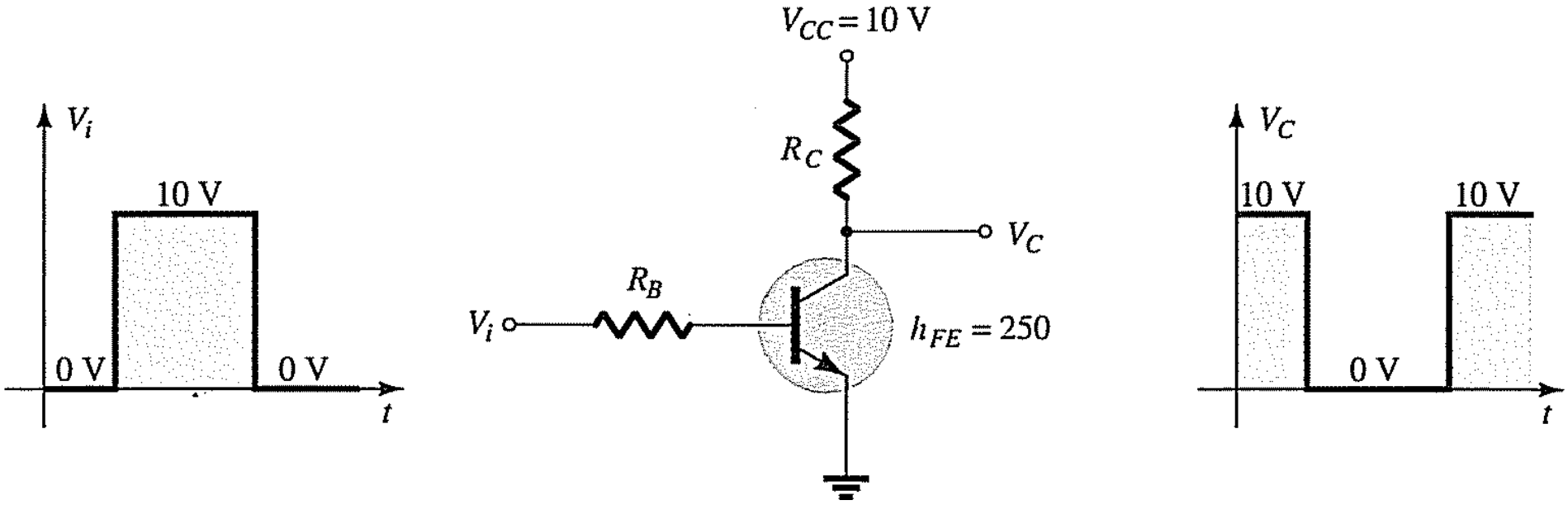


Transistor Switching Networks

- Because of V_E is grounded, so $V_{BE} = V_B = 0.7$
- For vin = 0: $$I_B = \frac{V_i - V_B}{R_B} = \frac{0 - 0.7}{68k} = -10.29\ \mu\text{A}$$
- I_B = -10.29 µA is way below I_B = 0 A in the load-line, so for sure it is in the cutoff-region
- Because of $V_{CE} = V_{CC}$ for cutoff-region, while $V_C = V_{CE}$ for this configuration, the output V_C will be 5 V
- For vin = 5: $$I_B = \frac{V_i - V_B}{R_B} = \frac{5 - 0.7}{68k} = 63.24\ \mu\text{A}$$
- I_B = 63.24 µA is way above I_B = 50 µ A in the load-line, so for sure it is in the saturation-region
- Because of V_{CE} = 0 for saturation-region, while $V_C = V_{CE}$ for this configuration, the output V_C will be 0 V

Example 4.24

- Determine R_B and R_C for the transistor inverter if I_{Csat} = 10 mA



Example 4.24

- At the saturation point, I_{Csat} is defined by:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

$$10m = \frac{10}{R_C}$$

$$\therefore R_C = 1\,\text{k}\Omega$$

- Obtaining I_B for saturation region:

$$I_{C_{sat}} = \beta I_B$$

$$10m = 250 I_B$$

$$\therefore I_B = 40\,\mu\text{A}$$

Example 4.24

- To make sure that I_B is really in the saturation region, use I_B greater than the I_B obtained at the saturation point. As for that, use I_B = 60 μA
- At saturation region, input voltage V_i must be high. As for that, V_i = 10 V
- Because V_E = 0 and V_{BE} = 0.7, the value of V_B = 0.7
- To obtain R_B:

$$I_B = \frac{V_i - V_B}{R_B}$$

$$60\mu = \frac{10 - 0.7}{R_B}$$

$$\therefore R_B = 155\,\text{k}\Omega\,(\text{use}\,150\,\text{k}\Omega)$$

Example 4.24

- Use 150 kΩ due to 155 kΩ is not exist in the real world
- Check back whether 150 kΩ can be used for transistor switching network:

$$I_B = \frac{V_i - V_B}{R_B} = \frac{10 - 0.7}{150k} = 62\ \mu\text{A}$$

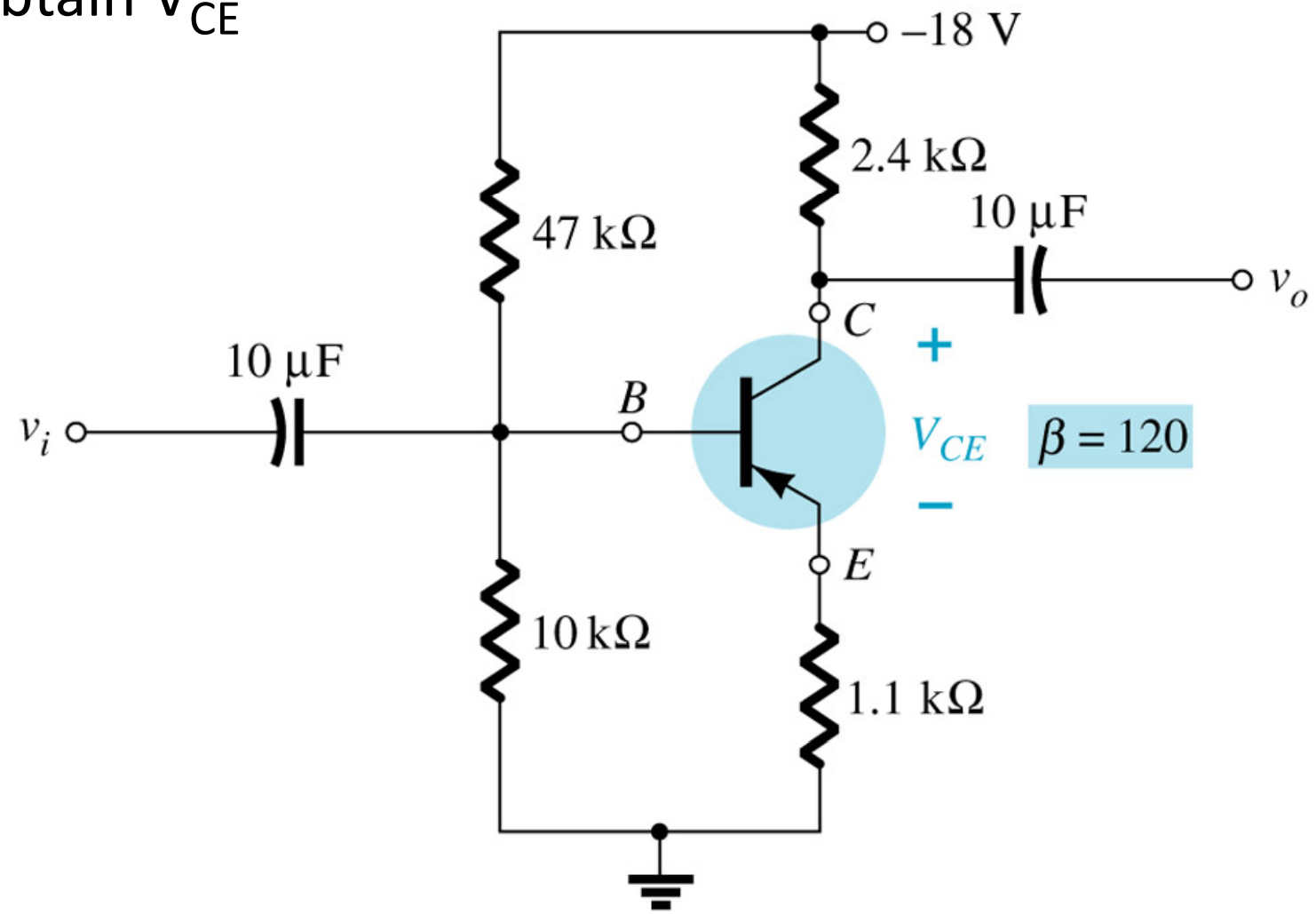
- The saturation point is at I_B = 40 μA, so the use of 150 kΩ is appropriate because the IB produced is surely in the saturation region

pnp Transistors

- Note that all the analysis and techniques explained is only involving *npn* transistors
- Therefore for *pnp* transistor, all of the analysis and techniques learned can also be applied because of the total current flowing in and out of the transistor is still the same as in *npn* that is $I_E = I_B + I_C$
- The only difference between *npn* and *pnp* transistor is the direction of the current flows in and out of the transistor

Example 4.27

- Obtain V_{CE}



Example 4.27

- By examining the circuit given, it is a voltage-divider bias configuration
- As for that, approximate analysis can be done if the condition are satisfied:

$$\beta R_E = (120)(1.1k) = 132\,\text{k}\Omega$$

$$10R_2 = 10(10k) = 100\,\text{k}\Omega$$

$$\therefore \beta R_E \geq 10R_2$$

- The condition are satisfied, approximate analysis can be used:

$$E_{TH} = V_B$$

Example 4.27

- Because of the value of V_{CC} is negative, the current will flows from ground to V_{CC} resulting in:

$$\frac{0-V_B}{10k}=\frac{V_B-(-18)}{47k}$$

$$\therefore V_B=-3.16\,\mathrm{V}$$

- As for the current flows in pnp transistor has been the reversed as in npn transistor, the diode voltage drop for p-n junction will be:

$$V_{EB}=V_E-V_B=0.7$$

- As for that, V_E is obtained:

$$0.7=V_E-(-3.16)$$

$$\therefore V_E=-2.46\,\mathrm{V}$$

Example 4.27

- For I_E:

$$I_E = \frac{0 - V_E}{1.1k} = \frac{-(-2.46)}{1.1k} = 2.24\,\text{mA}$$

- As for $I_C \approx I_E$, V_C is obtained:

$$I_C = \frac{V_C - V_{CC}}{R_C}$$

$$2.24\,\text{mA} = \frac{V_C - (-18)}{2.4k}$$

$$\therefore V_C = -12.62\,\text{V}$$

Example 4.27

- Finally, V_{CE} is obtained:

$$V_{CE} = V_C - V_E = -12.62 - (-2.46) = -10.16\ \text{V}$$

Transistor Hints and Tips

- All the transistor current (I_B, I_C and I_E) must be in positive values due to the current flows in and out of the transistor must be satisfied, $I_E = I_B + I_C$
- The base current I_B must be small (in μA) to ensure that the equation $I_C \approx I_E$ is satisfied